CERTIFICATE

I, Kazutaka TERASAKI, residing at #102, 1-27-3, Kizuki, Nakahara-ku, Kawasaki-shi, Kanagawa-ken, 211-0025 Japan, hereby certify that I am the translator of the attached document, namely a Certified Copy of Japanese Patent Application No. 2002-277956 and certify that the following is a true translation to the best of my knowledge and belief.

Kazutaka Terasaki August 23, 2007

Signature of Translator Date

[Name of Document] SPECIFICATION

[Title of the Invention] ELECTRONIC CIRCUIT, ELECTRO-OPTICAL DEVICE, METHOD OF DRIVING ELECTRO-OPTICAL DEVICE, AND ELECTRONIC APPARATUS

[Claims]

[Claim 1] An electronic circuit comprising:

an electronic element;

a capacitor for accumulating an amount of charge corresponding to a voltage value corresponding to a data signal; and

a first transistor whose conduction state is controlled according to the amount of charge accumulated in the capacitor, the first transistor supplying an amount of current corresponding to the conduction state to the electronic element;

wherein the capacitor is capable of accumulating an amount of charge corresponding to a data signal regardless of whether a data current or a data voltage is supplied as the data signal.

[Claim 2] The electronic circuit according to Claim 1,

wherein the data current as the data signal is a multi-value data current and the data voltage as the data signal is a binary data voltage, and

wherein the multi-value data current and the binary data voltage can be supplied to the capacitor via a second

transistor.

[Claim 3] The electronic circuit according to Claim 1 or 2,

wherein a third transistor is connected between a gate and a drain of the first transistor, the third transistor exhibiting a conduction state based on the data current and being provided for compensation of a threshold voltage of the first transistor.

[Claim 4] The electronic circuit according to any one of Claims 1 to 3, further comprising:

a fourth transistor for determining a timing for driving electronic element in a conduction state based on the data signal.

[Claim 5] An electronic circuit comprising:

an electronic element;

a capacitor that is capable of accumulating an amount of charge corresponding to a data signal regardless of whether a data current or a data voltage is supplied as the data signal;

a first transistor whose conduction state is controlled according to the amount of charge accumulated in the capacitor, the first transistor supplying an amount of current corresponding to the conduction state to the electronic element; and

a fifth transistor for resetting the amount of charge

held in the capacitor when the fifth transistor is turned on.

[Claim 6] The electronic circuit according to any one of Claims 1 to 5,

wherein the electronic element is an electro-optical element.

[Claim 7] The electronic circuit according to Claim 6,

wherein the electro-optical element is an EL element.

[Claim 8] The electronic circuit according to Claim 7,

wherein the EL element has a light-emitting layer composed of an organic material.

[Claim 9] An electro-optical device including a plurality of scanning lines, a plurality of data lines, and a plurality of unit circuits, the electro-optical device comprising:

a data-voltage outputting circuit that outputs binary data voltages as data signals individually to the plurality of unit circuits via the plurality of data lines; and

a data-current outputting circuit that outputs data currents individually to the plurality of unit circuits to the plurality of data lines.

[Claim 10] The electro-optical device according to Claim 9,

wherein the data voltages and the data currents are supplied via common data lines.

[Claim 11] The electro-optical device according to Claim 9,

wherein the data voltages and the data currents are supplied via different data lines.

[Claim 12] An electro-optical device comprising:

a plurality of scanning lines;

a plurality of data lines crossing the plurality of scanning lines; and

a plurality of unit circuits provided in association with intersections of the plurality of scanning lines and the plurality of data lines, the plurality of unit circuits driving supplying driving currents to electro-optical elements, the driving currents corresponding to data signals supplied via the plurality of data lines;

wherein controlling means is provided for generating and outputting either binary data voltages for exercising digital gray scale on the electro-optical elements according to image data or multi-value data currents for exercising analog data currents on the electro-optical elements according to image data.

[Claim 13] The electro-optical device according to Claim 12,

wherein each of the plurality of unit circuits includes:

a capacitor for accumulating an amount of charge

corresponding to a voltage value corresponding to a data signal; and

a first transistor whose conduction state is controlled according to the amount of charge accumulated in the capacitor, the first transistor supplying an amount of current corresponding to the conduction state to the electronic element;

wherein the capacitor is capable of accumulating an amount of charge corresponding to a data signal regardless of whether a data current or a data voltage is supplied as the data signal.

[Claim 14] The electro-optical device according to Claim 12 or 13,

wherein the data current as the data signal is a multi-value data current and the data voltage as the data signal is a binary data voltage, and

wherein the multi-value data current and the binary data voltage can be supplied to the capacitor via a second transistor.

[Claim 15] The electro-optical device according to any one of Claims 12 to 14,

wherein a third transistor is connected between a gate and a drain of the first transistor, the third transistor exhibiting a conduction state based on the data current and being provided for compensation of a threshold voltage of

the first transistor.

[Claim 16] The electro-optical device according to any one of Claims 12 to 15,

wherein each of the plurality of unit circuits includes a fourth transistor for determining a timing for driving the electro-optical element in a conduction state based on the data signal.

[Claim 17] The electro-optical device according to any one of Claims 12 to 16,

wherein each of the plurality of unit circuits includes a fifth transistor for resetting the amount of charge held in the capacitor when the fifth transistor is turned on.

[Claim 18] The electro-optical device according to any one of Claims 12 to 17,

wherein the controlling means drives the electro-optical elements by generating binary data voltages for exercising digital gray scale on the electro-optical elements in a low-power-consumption mode while generating multi-value data currents for exercising analog data currents on the electro-optical elements in a non-low-power-consumption mode.

[Claim 19] The electro-optical device according to any one of Claims 12 to 17,

wherein the controlling means drives the electro-optical elements by generating binary data voltages for

exercising digital gray scale on the electro-optical elements when the image data is first display data while generating multi-value data currents for exercising analog data currents on the electro-optical elements when the image data is second display data having a higher display quality than the first display data.

[Claim 20] The electro-optical device according to Claim 18 or 19,

wherein the controlling means includes:

a data-voltage generating circuit that generates binary data voltages for exercising digital gray scale on the electro-optical elements; and

a data-current generating circuit that generates multi-value data currents for exercising analog gray scale on the electro-optical elements.

[Claim 21] The electro-optical device according to Claim 20,

wherein a data-voltage outputting circuit that outputs the binary data voltages from the data-voltage generating circuit and a data-current outputting circuit that outputs the multi-value data currents from the data-current generating circuit are provided between the controlling means and each of the plurality of data lines, and a switching circuit that outputs either the binary data voltages from the data-voltage generating circuit or the

multi-value data currents from the data-current generating circuit to the data line is provided.

[Claim 22] The electro-optical device according to any one of Claims 12 to 21,

wherein the digital gray scale is time-division gray scale.

[Claim 23] The electro-optical device according to Claim 22,

wherein the time-division gray scale is exercised by writing the binary data voltages to the unit circuits associated with one selected scanning line, starting supply of currents having current levels corresponding to the binary data voltages to the electro-optical elements, and stopping the supply of currents to the electro-optical elements after a predetermined time.

[Claim 24] The electro-optical device according to any one of Claims 12 to 23,

wherein the electro-optical elements are EL elements.

[Claim 25] The electro-optical device according to Claim 24,

wherein each of the EL elements has a light-emitting layer composed of an organic material.

[Claim 26] A method of driving an electro-optical device including:

a plurality of scanning lines;

a plurality of data lines crossing the plurality of scanning lines; and

a plurality of unit circuits provided in association with intersections of the plurality of scanning lines and the plurality of data lines, the plurality of unit circuits driving supplying driving currents to electro-optical elements, the driving currents corresponding to data signals supplied via the plurality of data lines;

wherein the electro-optical elements are driven by generating binary data voltages for exercising digital gray scale on the electro-optical elements in a low-power-consumption mode while generating multi-value data currents for exercising analog data currents on the electro-optical elements in a non-low-power-consumption mode.

[Claim 27] A method of driving an electro-optical device including:

a plurality of scanning lines;

a plurality of data lines crossing the plurality of scanning lines; and

a plurality of unit circuits provided in association with intersections of the plurality of scanning lines and the plurality of data lines, the plurality of unit circuits driving supplying driving currents to electro-optical elements, the driving currents corresponding to data signals supplied via the plurality of data lines;

wherein the electro-optical elements are driven by generating binary data voltages for exercising digital gray scale on the electro-optical elements when the image data is first display data while generating multi-value data currents for exercising analog data currents on the electro-optical elements when the image data is second display data having a higher display quality than the first display data.

[Claim 28] The method of driving an electro-optical device according to Claim 26 or 27,

wherein the digital gray scale is time-division gray scale.

[Claim 29] The method of driving an electro-optical device according to Claim 28,

wherein the time-division gray scale is exercised by writing the binary data voltages to the unit circuits associated with one selected scanning line, starting supply of currents having current levels corresponding to the binary data voltages to the electro-optical elements, and stopping the supply of currents to the electro-optical elements after a predetermined time.

[Claim 30] The method of driving an electro-optical device according to any one of Claims 26 to 29,

wherein the electro-optical elements are EL elements.

[Claim 31] The method of driving an electro-optical device according to Claim 30,

wherein each of the EL elements has a light-emitting layer composed of an organic material.

[Claim 32] An electronic apparatus comprising the electro-optical device according to any one of Claims 9 to 25.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The present invention relates to electronic circuits, electro-optical devices, methods of driving electro-optical devices, and electronic apparatuses.

[0002]

[Description of the Related Art]

Recently, in the field of display devices as electro-optical devices, interests have arisen for electro-optical devices including organic EL elements. In an electro-optical device of this type, analog gray scale is used as a driving method for controlling halftones of organic EL elements (e.g., refer to Patent Document 1). In a method of analog gray scale, a voltage between the source and gate of a driving transistor for supplying a current having a current level corresponding to a multi-value data current to an organic EL element is used as a threshold voltage of the driving transistor. According to this method, a current supplied from a DA converter circuit in accordance with a

luminance level (data current) is accumulated in a hold capacitor of a pixel circuit. A charge voltage corresponding to the amount of charge accumulated in the hold capacitor is applied to the gate of the driving transistor implemented by a thin-film transistor (TFT). The driving transistor supplies a driving current in accordance with the charge voltage corresponding to the data current to the organic L element.

[0003]

[Patent Document 1]

JP-A-2001-147659

[0004]

[Problems to be Solved by the Invention]

In the DA converter circuit that is used in the current programming method, implementation by thin-film transistors (TFTs) adopted for the pixel circuits has been difficult due to the problem of precision, so that it has been common to use an external IC driver.

[0005]

However, a DA converter circuit that is implemented by an external IC driver has had a problem that power consumption is larger compared with a TFT driver circuit that is formed on a display panel. In view of this problem, digital gray scale is a possible approach, since a DA converter circuit for generating multi-values (analog

values) is not needed and therefore power consumption can be reduced. However, unfortunately, the display quality achieved with digital gray scale is lower than that achieved with analog gray scale.

[0006]

The present invention has been made in order to overcome the problem described above, and it is an object thereof to provide an electronic circuit, an electro-optical device, a method of driving an electro-optical device, and an electronic apparatus with which low power consumption and adequate display quality can be achieved simultaneously.

[0007]

[Means for Solving the Problems]

An electronic circuit according to the present invention includes an electronic element; a capacitor for accumulating an amount of charge corresponding to a voltage value corresponding to a data signal; and a first transistor whose conduction state is controlled according to the amount of charge accumulated in the capacitor, the first transistor supplying an amount of current corresponding to the conduction state to the electronic element; wherein the capacitor is capable of accumulating an amount of charge corresponding to a data signal regardless of whether a data current or a data voltage is supplied as the data signal.

[0008]

Accordingly, data voltages and data currents are used selectively, so that, for example, representation of halftones in two ways, such as digital gray scale and analog gray scale, is allowed. Thus, for example, for representation of halftones, digital gray scale is selected when low power consumption is more important than display quality while analog gray scale is selected when a high display quality is needed.

[0009]

In the electronic circuit, the data current as the data signal is a multi-value data current and the data voltage as the data signal is a binary data voltage, and the multi-value data current and the binary data voltage can be supplied to the capacitor via a second transistor.

[0010]

In this case, for example, when the digital gray scale and analog gray scale are used, binary data voltages for digital gray scale and multi-value data currents for analog gray scale are supplied individually to the capacitor via the second switching transistor.

[0011]

In the electronic circuit, a third transistor is connected between a gate and a drain of the first transistor, the third transistor exhibiting a conduction state based on the data current and being provided for

compensation of a threshold voltage of the first transistor.

[0012]

In this case, the third transistor can be used to compensate for manufacturing variation of the threshold voltage of the first transistor. Thus, the fist transistor exhibits a conduction state corresponding to a multi-value data current without being affected by the threshold voltage.

[0013]

In the electronic circuit, a fourth transistor for determining a timing for driving electronic element in a conduction state based on the data signal is provided.

In this case, the fourth transistor starts driving the electronic element by supplying an amount of current corresponding to the conduction state based on the multi-value data current.

[0014]

An electronic circuit according to the present invention includes an electronic element; a capacitor that is capable of accumulating an amount of charge corresponding to a data signal regardless of whether a data current or a data voltage is supplied as the data signal; a first transistor whose conduction state is controlled according to the amount of charge accumulated in the capacitor, the first transistor supplying an amount of current corresponding to

the conduction state to the electronic element; and a fifth transistor for resetting the amount of charge held in the capacitor when the fifth transistor is turned on.

[0015]

In this case, the binary data voltage held by the capacitor is reset by the fifth transistor, and the capacitor waits for supply of a next binary data voltage.

In the electronic circuit, the electronic element is an electro-optical element.

[0016]

In this case, the electro-optical element emits light in accordance with the conduction state of the first transistor.

In the electronic circuit, the electro-optical element is an EL element.

[0017]

In this case, the EL element emits light in accordance with the conduction state of the first transistor.

In the electronic circuit, the EL element has a light-emitting layer composed of an organic material.

[0018]

In this case, the EL element is an organic EL element having a light-emitting layer composed of an organic material.

An electro-optical device according to the present

invention is an electro-optical device including a plurality of scanning lines, a plurality of data lines, and a plurality of unit circuits, the electro-optical device including a data-voltage outputting circuit that outputs binary data voltages as data signals individually to the plurality of unit circuits via the plurality of data lines; and a data-current outputting circuit that outputs data currents individually to the plurality of unit circuits to the plurality of data lines.

[0019]

Accordingly, digital gray scale can be exercised when binary data voltages are input from the data-voltage outputting circuit, while analog gray scale can be exercised when multi-level data currents are input from the data-current outputting circuit.

[0020]

In the electro-optical device, the data voltages and the data currents are supplied via common data lines.

In this case, when digital gray scale is exercised and when analog gray scale is exercised, binary data voltages and multi-level data currents are supplied via common data lines.

[0021]

In the electro-optical device, the data voltages and the data currents are supplied via different data lines.

In this case, when digital gray scale is exercised and when analog gray scale is exercised, binary data voltages and multi-level data currents are supplied to the unit circuits via separate data lines.

[0022]

An electro-optical device according to the present invention includes a plurality of scanning lines; a plurality of data lines crossing the plurality of scanning lines; and a plurality of unit circuits provided in association with intersections of the plurality of scanning lines and the plurality of data lines, the plurality of unit circuits driving supplying driving currents to electro-optical elements, the driving currents corresponding to data signals supplied via the plurality of data lines; wherein controlling means is provided for generating and outputting either binary data voltages for exercising digital gray scale on the electro-optical elements according to image data or multi-value data currents for exercising analog data currents on the electro-optical elements according to image data.

[0023]

Accordingly, the controlling means can represent halftones of the electro-optical elements in two ways, namely, digital gray scale and analog gray scale. Thus, for example, for representation of halftones, digital gray scale

is selected when low power consumption is more important than display quality while analog gray scale is selected when a high display quality is needed.

[0024]

In the electro-optical device, each of the plurality of unit circuits includes a capacitor for accumulating an amount of charge corresponding to a voltage value corresponding to a data signal; and a first transistor whose conduction state is controlled according to the amount of charge accumulated in the capacitor, the first transistor supplying an amount of current corresponding to the conduction state to the electronic element; wherein the capacitor is capable of accumulating an amount of charge corresponding to a data signal regardless of whether a data current or a data voltage is supplied as the data signal.

[0025]

Accordingly, data voltages and data currents are used selectively, so that, for example, representation of halftones in two ways, such as digital gray scale and analog gray scale, is allowed. Thus, for example, for representation of halftones, digital gray scale is selected when low power consumption is more important than display quality while analog gray scale is selected when a high display quality is needed.

[0026]

In the electro-optical device, the data current as the data signal is a multi-value data current and the data voltage as the data signal is a binary data voltage, and the multi-value data current and the binary data voltage can be supplied to the capacitor via a second transistor.

[0027]

In this case, for example, when the digital gray scale and analog gray scale are used, binary data voltages for digital gray scale and multi-value data currents for analog gray scale are supplied individually to the capacitor via the second switching transistor.

[0028]

In the electro-optical device, in each of the plurality of unit circuits, a third transistor is connected between a gate and a drain of the first transistor, the third transistor exhibiting a conduction state based on the data current and being provided for compensation of a threshold voltage of the first transistor.

[0029]

In this case, the third transistor can be used to compensate for manufacturing variation of the threshold voltage of the first transistor. Thus, the fist transistor exhibits a conduction state corresponding to a multi-value data current without being affected by the threshold voltage.

[0030]

In the electro-optical device, each of the plurality of unit circuits includes a fourth transistor for determining a timing for driving the electro-optical element in a conduction state based on the data signal is provided.

[0031]

In this case, the fourth transistor starts driving the electronic element by supplying an amount of current corresponding to the conduction state based on the multi-value data current.

[0032]

In the electro-optical device, each of the plurality of unit circuits includes a fifth transistor for resetting the amount of charge held in the capacitor when the fifth transistor is turned on.

In this case, the binary data voltage held by the capacitor is reset by the fifth transistor, and the capacitor waits for supply of a next binary data voltage.

[0033]

In the electro-optical device, the controlling means drives the electro-optical elements by generating binary data voltages for exercising digital gray scale on the electro-optical elements in a low-power-consumption mode while generating multi-value data currents for exercising analog data currents on the electro-optical elements in a

non-low-power-consumption mode.

[0034]

In this case, the controlling means can represent halftones of the electro-optical elements by digital gray scale in the low-power-consumption mode and in analog gray scale in the non-low-power-consumption mode.

[0035]

In the electro-optical device, the controlling means drives the electro-optical elements by generating binary data voltages for exercising digital gray scale on the electro-optical elements when the image data is first display data while generating multi-value data currents for exercising analog data currents on the electro-optical elements when the image data is second display data having a higher display quality than the first display data.

[0036]

In this case, the controlling means can represent halftones of the electro-optical elements by digital gray scale when a high display quality is not needed and in analog gray scale when a high display quality is needed.

[0037]

In the electro-optical device, the controlling means includes a data-voltage generating circuit that generates binary data voltages for exercising digital gray scale on the electro-optical elements; and a data-current generating

circuit that generates multi-value data currents for exercising analog gray scale on the electro-optical elements.

[0038]

In this case, the data-voltage generating circuit generates binary data voltages for exercising digital gray scale, and the data-current generating circuit generates multi-value data currents for exercising analog gray scale.

[0039]

In the electro-optical device, a data-voltage outputting circuit that outputs the binary data voltages from the data-voltage generating circuit and a data-current outputting circuit that outputs the multi-value data currents from the data-current generating circuit are provided between the controlling means and each of the plurality of data lines, and a switching circuit that outputs either the binary data voltages from the data-voltage generating circuit or the multi-value data currents from the data-current generating circuit to the data line is provided.

[0040]

In this case, the switching circuit outputs the binary data voltages from the data-voltage generating circuit to the data line when digital gray scale is exercised while outputting the multi-value data currents from the data-

current generating circuit to the data line when analog gray scale is exercised.

[0041]

In the electro-optical device, the digital gray scale is time-division gray scale.

In this case, halftones of the electro-optical elements are controlled by time-division gray scale.

In the electro-optical device, the time-division gray scale is exercised by writing the binary data voltages to the unit circuits associated with one selected scanning line, starting supply of currents having current levels corresponding to the binary data voltages to the electro-optical elements, and stopping the supply of currents to the electro-optical elements after a predetermined time.

[0042]

In this case, halftones of the electro-optical elements are controlled by writing the binary data voltages to the unit circuits associated with one selected scanning line, supplying currents having current levels corresponding to the binary data voltages to the electro-optical elements, and stopping the supply of currents to the electro-optical elements after a predetermined time.

[0043]

In the electro-optical device, the electro-optical element is an EL element.

In this case, the EL element emits light in accordance with the conduction state of the second transistor.

[0044]

In the electro-optical device, the EL element has a light-emitting layer composed of an organic material.

In this case, the EL element is an organic EL element having a light-emitting layer composed of an organic material.

[0045]

A method of driving an electro-optical device according to the present invention is a method of driving an electro-optical device including a plurality of scanning lines; a plurality of data lines crossing the plurality of scanning lines; and a plurality of unit circuits provided in association with intersections of the plurality of scanning lines and the plurality of data lines, the plurality of unit circuits driving supplying driving currents to electro-optical elements, the driving currents corresponding to data signals supplied via the plurality of data lines; wherein the electro-optical elements are driven by generating binary data voltages for exercising digital gray scale on the electro-optical elements in a low-power-consumption mode while generating multi-value data currents for exercising analog data currents on the electro-optical elements in a non-low-power-consumption mode.

[0046]

Accordingly, halftones of the electro-optical elements are controlled by digital gray scale in the low-power-consumption mode, while halftones of the electro-optical elements are controlled by analog gray scale in the non-low-power-consumption mode.

A method of driving an electro-optical device according to the present invention is a method of driving an electro-optical device including a plurality of scanning lines; a plurality of data lines crossing the plurality of scanning lines; and a plurality of unit circuits provided in association with intersections of the plurality of scanning lines and the plurality of data lines, the plurality of unit circuits driving supplying driving currents to electro-optical elements, the driving currents corresponding to data signals supplied via the plurality of data lines; wherein the electro-optical elements are driven by generating binary data voltages for exercising digital gray scale on the electro-optical elements when the image data is first display data while generating multi-value data currents for exercising analog data currents on the electro-optical elements when the image data is second display data having a higher display quality than the first display data.

[0047]

Accordingly, halftones of the electro-optical elements

are controlled by digital gray scale when a high display quality is not needed, while halftones of the electro-optical elements are controlled by analog gray scale when a high display quality is needed.

In the method of driving an electro-optical device, the digital gray scale is time-division gray scale.

[0048]

In this case, halftones of the electro-optical elements are controlled by time-division gray scale.

In the method of driving an electro-optical device, the time-division gray scale is exercised by writing the binary data voltages to the unit circuits associated with one selected scanning line, starting supply of currents having current levels corresponding to the binary data voltages to the electro-optical elements, and stopping the supply of currents to the electro-optical elements after a predetermined time.

[0049]

In this case, halftones of the electro-optical elements are controlled by writing the binary data voltages to the unit circuits associated with one selected scanning line, supplying currents having current levels corresponding to the binary data voltages to the electro-optical elements, and stopping the supply of currents to the electro-optical elements after a predetermined time.

[0050]

In the method of driving an electro-optical device, the electro-optical element is an EL element.

In this case, the EL element emits light in accordance with the conduction state of the first transistor.

[0051]

In the method of driving an electro-optical device, the EL element has a light-emitting layer composed of an organic material.

In this case, the EL element is an organic EL element having a light-emitting layer composed of an organic material.

[0052]

An electronic apparatus according to the present invention includes the electro-optical device according to any one of Claims 9 to 25.

Accordingly, the electronic apparatus can achieve low power consumption and adequate display quality simultaneously.

[0053]

[Description of the Embodiments]

(First Embodiment)

Now, a first embodiment of the present invention will be described with reference to Figs. 1 to 5.

[0054]

Fig. 1 shows a block circuit diagram showing the electrical configuration of an organic EL display 10 as an electro-optical device. Referring to Fig. 1, the organic EL display 10 is capable of representing halftones either by digital gray scale or analog gray scale. More specifically, in this embodiment, the digital gray scale is time-division gray scale. In the time-division gray scale, binary data voltages are written to pixel circuits associated with a selected scanning line, so that supply of currents having current levels corresponding to the binary data voltages to electro-optical elements is started. Then, supply of currents to the electro-optical elements is stopped after a predetermined time, thereby allowing representation of 64 gray scales. In the analog gray scale, gray scales are represented by a driving method in which gate-source voltages of driving transistors for supplying currents having current levels corresponding to multi-value data currents to organic EL elements are set to threshold voltages of the transistors.

[0055]

In the time-division gray scale in this embodiment, as shown in Fig. 3, scanning for displaying a single image (one frame) is divided into six sub-frames SF1 to SF6. In each of the sub-frames SF1 to SF6, the scanning lines are selected sequentially, and the luminance of each of the

organic EL elements of the pixel circuits connected to the selected scanning line is set to either a light-emitting state or a non-light-emitting state on the basis of binary voltage data, and the organic EL elements are individually caused to enter the non-light emitting state sequentially after a predetermined period.

[0056]

The sub-frames SF1 to SF6 have light-emitting periods (light-emitting times) TL1 to TL6, respectively, and the light-emitting periods TL1 to TL6 are set such that:

$$32TL1 = 16TL2 = 8TL3 = 4TL4 = 2TL5 = TL6$$

That is, the time ratio among the light-emitting periods is set such that:

$$TL1:TL2:TL3:TL4:TL5:TL6 = 1:2:4:8:16:32$$

[0057]

A luminance level of "7" can be achieved by driving the pixel circuit so that the organic EL element is caused to emit light in the first to third sub-frames SF1 to SF3 while deactivating the pixel circuit so that the organic EL element is caused to refrain from emitting light in the fourth to sixth sub-frames SF4 to SF6.

[0058]

A luminance level of "32" can be achieved by driving the pixel circuit so that the organic EL element is caused to emit light is the sixth sub-frame SF6 while deactivating

the pixel circuit so that the organic EL element is caused to refrain from emitting light in the first to the fifth sub-frames SF1 to SF5.

[0059]

A luminance level of "44" can be achieved by driving the pixel circuit so that the organic EL element is caused to emit light is the third, fourth, and sixth sub-frames SF3, SF4, and SF6 while deactivating the pixel circuit so that the organic EL element is caused to refrain from emitting light in the first, second, and fifth sub-frames SF1, SF2, and SF5.

[0060]

By selecting the subframes SF1 to SF6 appropriately on a frame-by-frame basis, halftones can be achieved.

Referring to Fig. 1, the organic EL display 10 includes a display panel 11, a scanning-line driving circuit 12, a data-line driving circuit 13, and a control circuit 14.

[0061]

The display panel 11, the scanning-line driving circuit 12, the data line driving circuit 13, and the control circuit 14 of the organic EL display 10 may be implemented individually by independent electronic components. For example, the scanning-line driving circuit 12, the data-line driving circuit 13, and the control circuit 14 may be implemented by single-chip semiconductor integrated

circuits. Alternatively, part of or the entire display panel 11, scanning-line driving circuit 12, data-line driving circuit 13, and control circuit 14 may be implemented by an integrated electronic component. For example, the data-line driving circuit 13 and the scanning-line driving circuit 12 may be formed integrally with the display-panel 11. Alternatively, part of or the entire scanning-line driving circuit 12, data-line driving circuit 13, and control circuit 14 may be implemented by a programmable IC chip, with the functions of these components implemented in software by a program written to the IC chip.

[0062]

As shown in Fig. 1, the display panel 11 includes pixel circuits 20 as a plurality of electronic circuits or unit circuits, arranged in a matrix form. That is, the pixel circuits 20 are disposed in association with intersections of a plurality of (m) data lines X1 to Xm (where m is an integer) extending in a column direction, and a plurality of (n) scanning lines Y1 to Yn (where n is an integer) extending in a row direction. The pixel circuits are individually connected between the associated data lines X1 to Xm and scanning lines Y1 to Yn, and are arranged to form a matrix. Each of the pixel circuits 20 includes an organic EL element 21 (refer to FIG. 2) having a light-emitting layer composed of an organic material, as an electronic

element or an electro-optical element. Transistors provided in the pixel circuit 20, described later, are usually implemented by thin-film transistors (TFTs).

[0063]

Fig. 2 shows an electric circuit diagram for explaining the internal circuit configuration of the pixel circuits 20. For the convenience of description, the pixel circuit 20 disposed at the intersection of the m-th data line Xm and the n-th scanning line Yn and connected between the data line Xm and the scanning line Yn will be described.

[0064]

The pixel circuit 20 includes a first switching transistor Q1, a second switching transistor Q2, a driving transistor Q3, a converting transistor Q4, a resetting transistor Q5, and a hold capacitor C1 as a capacitor. The first and second switching transistors Q1 and Q2 and the resetting transistor Q5 are implemented by N-channel FETs. The driving transistor Q3 and the converting transistor Q4 are implemented by P-channel FETs.

[0065]

The drain of the driving transistor Q3 is connected to the anode of the organic EL element 21, and the source thereof is connected to a power-supply line L1. To the power-supply line L1, a power-supply voltage VOEL for driving the organic EL element 21 is supplied. The gate of

the driving transistor Q3 is connected to a first end of the hold capacitor C1, and the first end of the hold capacitor C1 is connected to the data line Xm via the first switching transistor Q1. To a second end of the hold capacitor C1, the power-supply voltage VOEL is applied via the power-supply line L1. The gate of the driving transistor Q3 is connected to the gate of the converting transistor Q4. To the source of the converting transistor Q4, the power-supply voltage VOEL is applied via the power-supply line L1.

[0066]

The second switching transistor Q2 is connected between the gate and drain of the converting transistor Q4. Thus, the drain of the converting transistor Q4 is connected to the data line Xm via the second switching transistor Q2 and the first switching transistor Q1. As a result, the transistors Q1, Q2, Q3, and Q4 form a current mirror circuit. Ideally, a current that flows through the transistor Q4 is decreased or increased proportionally according to a size ratio between the transistor Q3 and the transistor Q4 and a resulting current flows through the transistor Q3.

[0067]

The gate of the first switching transistor Q1 is connected to a first sub-scanning line Yn1 of the scanning line Yn, and it receives a first scanning signal SCn1 via

the first sub-scanning line Yn1. The gate of the second switching transistor Q2 is connected to a second sub-scanning line Yn2 of the scanning line Yn, and it receives a second scanning signal SCn2 via the second sub-scanning line Yn2. The first switching transistor Q1 and the second switching transistor Q2 are turned on or off according to the first scanning signal SCn1 and the second scanning signal SCn2, respectively, as will be described later. Then, digital data VDGDATAm or an analog data current IANDATAm supplied via the data line Xm, described later, is supplied to the hold capacitor C1.

[0068]

The resetting transistor Q5 is connected between the ends of the hold capacitor C1. The gate of the resetting transistor Q5 is connected to a third sub-scanning line Yn3 of the scanning line Yn, and it receives a third scanning signal SCn3 via the third sub-scanning line Yn3. When the resetting transistor Q5 is turned on according to the third scanning signal SCn3, the power-supply voltage VOEL supplied via the power-supply line L1 is applied to the first end of the hold capacitor C1 via the resetting transistor Q5. When the power-supply voltage VOEL is applied to the first end of the hold capacitor C1, the hold capacitor C1 is reset, whereby the driving transistor Q3 is turned off.

[0069]

In this embodiment, the first switching transistor Q1 functions as a second transistor, the driving transistor Q3 functions as a first transistor, the converting transistor Q4 functions as a third transistor, and the resetting transistor Q5 functions as a fifth transistor.

[0070]

In the pixel circuit 20 configured as described above, light emission by the organic EL element 21 can be controlled by inputting a binary data voltage or a multi-value data current.

In the pixel circuits 20, binary data voltages are written to pixel circuits associated with a selected scanning line sequentially selected, and supply of currents having current levels corresponding to the binary data voltages to the organic EL elements 21 is started. Then, supply of currents to the organic EL elements 21 is stopped after a predetermined time, thereby achieving time-division gray scale.

[0071]

As shown in Fig. 4, in the subframes SF1 to SF6, the second switching transistor Q2 and the resetting transistor Q5 are kept turned off according to the second and third scanning signals SCn2 and SCn3 at L level. In this state, the first switching transistor Q1 is turned on according to the first scanning signal SCn1 at H level, so that digital

data VDGDATAm output from a digital-data-voltage output circuit is supplied to the pixel circuit 20 shown in Fig. 2 via the data line Xm. Thus, an amount of charge corresponding to the binary voltage data is accumulated in the hold capacitor C1.

[0072]

The conduction state of the driving transistor Q3 is set in accordance with the amount of charges corresponding to the voltage data and accumulated in the hold capacitor C1, and the organic EL element 21 is caused to emit light at a corresponding luminance. At least within the light-emitting period of the organic EL element 21, preferably, the first scanning signal SCn1 is pulled to L level so that the first switching transistor Q1 is turned off. Each subframe at the pixels associated with each scanning line is finished by maintaining the third scanning signal SCn3 at H level for a predetermined period so that the resetting transistor Q5 is turned on. That is, the potential of the power-supply line L1 is applied to the first end of the hold capacitor C1, so that the data written to the hold capacitor C1 is set, whereby a current is inhibited from flowing through the driving transistor Q3. Thus, halftones can be represented by digital gray scale.

[0073]

The amount of charges causes a gate voltage at the gate

of the driving transistor Q3 and thereby determines the conduction state of the driving transistor Q3. However, preferably, for example, each of the binary voltage data is set so that the resistances of the driving transistor Q3 correspond to a minimum value and a maximum value, i.e., a minimum value and a maximum value of luminance of the organic EL element 21. When the driving transistor Q3 is implemented by a thin-film transistor, the saturation region is not necessarily clear. In that case, the binary voltage data may be set correspondingly to a lower limit value and an upper limit value of a desired range of luminance.

[0074]

More specifically, with the second switching transistor Q2 kept turned off, when the scanning signal SCn1 at H level is output to the first subscanning line Yn1, the switching transistor Q1 is turned on. When the fist switching transistor Q1 is turned on, digital data VDGDATAm is supplied to the hold capacitor C1 via the data line Xm. The digital data VDGDATAm is binary data, i.e., data for setting either a minimum value or a maximum value (or a lower limit value or an upper limit value) of luminance of the organic EL element 21, so that the resistance of the driving transistor Q3 becomes either a minimum value or a maximum value. The holding capacitor C1 holding the digital data VDGDATAm holds the digital data VDGDATAm that has been

stored even when the scanning signal SCn1 is lost and the switching transistor Q1 is turned off.

[0075]

The driving transistor Q3 is controlled so that it is turned on or off according to the content of the digital data VDGDATAm stored. When the driving transistor Q3 is on, a driving current is supplied to the organic EL element 21 so that the organic EL element 21 is caused to emit light. On the other hand, when the driving transistor Q3 is off, supply of a driving current to the organic EL element 21 is stopped so that the organic EL element 21 is caused to stop emitting light.

[0076]

Then, at the ends of subframes, when the third scanning signal SCn3 is output to the third subscanning line Yn3 at a timing corresponding to each of the subframes SF1 to SF6, the resetting transistor Q5 that has been off is turned on. When the resetting transistor Q5 is turned on, the power-supply voltage VOEL is applied to the hold capacitor C1 via the resetting transistor Q5, so that the digital data VDGDATAm is deleted and the gate of the driving transistor Q3 is pulled to the potential of the power-supply voltage VOEL. That is, the hold capacitor C1 is reset.

[0077]

When the hold capacitor C1 is reset, the driving

transistor Q3 is turned off, so that the organic EL element 21 that has been emitting light according to the digital data VDGDATAm stops emitting light, and waits for a light emitting operation that is to be executed next. That is, when time-division gray scale by sequential light emission and simultaneous deletion is executed, in the light-emitting periods TL1 to TL6 of the organic EL element 21 of each of the pixel circuits 20, light is emitted during a period between the output of the first scanning signal SCn1 and the output of the third scanning signal SCn3.

[0078]

Analog gray scale for controlling the conduction state of the driving transistor Q3 in accordance with a gray scale, the driving transistor Q3 supplying a current having a current level corresponding to a multi-value data current to the organic EL element 21, is executed in the pixel circuit 20 in the following manner. As shown in Fig. 5, halftones can be represented by analog gray scale by outputting the first and second scanning signals SCn1 and SCn2 that controls ON/OFF of the first and second switching transistors Q1 and Q2 at specific timings. At this time, in order to maintain the resetting transistor Q5, the third scanning signal SCn3 at L level is output.

[0079]

That is, when the scanning signals SCn1 and SCn2 are

output to the first and second subscanning lines Yn1 and Yn2, the first and second switching transistors Q1 and Q2 are both turned on. Thus, an analog data current IANDATAm is supplied from the data line Xm via the first and second switching transistors Q1 and Q2. At this time, the gate voltage of the converting transistor Q4 has a voltage level corresponding to the analog data current IANDATAm, and the voltage level is held by the hold capacitor C1.

[0080]

As a result, the voltage applied to the gate of the driving transistor Q3 has a voltage level based on the analog data current IANDATAm, so that the driving transistor Q3 supplies an amount of current corresponding to the analog data current IANDATAm to the organic EL element 21. That is, a driving current that is proportional to the analog data current IANDATAm is supplied to the organic EL element 21, so that the organic EL element 21 starts emitting light at a gray scale corresponding to the analog data current IANDATAm.

[0081]

The scanning-line driving circuit 12 is a circuit for selecting one of the plurality of scanning lines Y1 to Yn, i.e., outputting a scanning signal, and driving the pixel circuits 20 connected to the selected scanning line. The scanning-line driving circuit 12 outputs scanning signals

SC1 to Sn respectively to the scanning lines Y1 to Yn at specific timings according to various signals.

[0082]

More specifically, in the time-division gray scale described earlier, in each of the subframes SF1 to SF6 of one frame, the pixel circuits on the individual scanning lines Y1 to Yn need to be driven sequentially. Thus, in order to display an image of one frame, during the period of each of the subframes SF1 to SF6, the scanning-line driving circuit 12 sequentially generates and outputs the scanning lines SC1 to SCn so that the scanning lines Y1 to Yn are selected sequentially. Then, the scanning-line driving circuit 12 outputs the scanning signals SC11 to SCn1 at H level to the first subscanning lines of the scanning lines Y1 to Yn individually for a predetermined period. After the elapse of the predetermined period, the scanning-line driving circuit 12 outputs the scanning signals SC13 to SCn3 at H level to the third subscanning lines Y13 to Yn3 of the associated scanning lines Y1 to Yn individually for a predetermined period.

[0083]

That is, in each of the subframes SF1 to SF6, light is emitted (light emission is refrained according to digital data) during the light-emitting periods TL1 to TL6, respectively.

In the analog gray scale described earlier, the scanning-line driving circuit 12 outputs the scanning signals SC11 to SCn1 and SC12 to SCn2 at H level respectively to the scanning lines Y1 to Yn at specific timings according to various signals supplied from the control circuit 14 as described earlier.

[0084]

The data-line driving circuit 13 includes a digital-data-voltage output circuit 13a as a data-voltage output circuit and an analog-data-current output circuit 13b as a data-current output circuit for each of the data lines X1 to Xm, as shown in Fig. 2. The digital-data-voltage output circuit 13a receives input of the digital data VDGDATA1 to VDGDATAm from the control circuit 14, and outputs the digital data VDGDATA1 to VDGDATAm to the associated data lines X1 to Xm via first switches Q11 in synchronization with the scanning signals SC11 to SCn1.

[0085]

The analog-data-current output circuit 13b receives input of the analog data currents IANDATA1 to IANDATAm from the control circuit 14. Thus, the analog-data-current output circuit 13b outputs the analog data currents IANDATA1 to IANDATAm to the associated data lines X1 to Xm via second switches Q12 in synchronization with the scanning signals SC11 to SCn1 and SC12 to SCn2.

[0086]

The first switches Q11 and the second switches Q12 constituting switching circuits are switches that select either the digital data VDGDATA1 to VDGDATAm or the analog data currents IANDATA1 to IANDATAm and output the digital data VDGDATA1 to VDGDATAm or the analog data currents IANDATA1 to IANDATAm to the data lines X1 to Xm. The first switches Q11 and the second switches S12 are implemented by N-channel FETs. The first switches Q11 are turned on when a first control signal SG1 is input from the control circuit 14 to the gate terminals thereof, and output the digital data VDGDATA1 to VDGDATAm to the data lines X1 to Xm. The second switches Q12 are turned on when a second control signal SG2 is input from the control circuit 14 to the gate terminals thereof, and outputs the analog data currents IANDATA1 to IANDATAm to the data lines X1 to Xm.

[0087]

That is, when a scanning signal is output to one scanning line by the scanning-line driving circuit 12, in the case of digital gray scale, the data-line driving circuit 13 outputs the digital data VDGDATA1 to VDGDATAm to the pixel circuits 20 on the selected scanning line. In the case of analog gray scale, the data-line driving circuit 13 outputs the analog data currents IANDATA1 to IANDATAm to the pixel circuits 20 on the selected scanning line.

[0088]

The control circuit 14 as controlling means, a data-voltage generating circuit, or a data-current generating circuit receives input of image data D from an external device that is not shown, and determines on the basis of the image data D whether halftones are to be controlled by digital gray scale or analog gray scale. In this embodiment, preferably, when the image data D does not require multi-level display, as in the case of text or the like as first display data, the digital data VDGDATA1 to VDGDATAm is generated to control halftones by digital gray scale. When the image data D requires multi-level display, as in the case of animation or movies as second display data, the analog data currents IANDATA1 to IANDATAm are generated to control halftones by analog gray scale. That is, the scanning-line driving circuit 12 and the data-line driving circuit 13 are controlled so that digital gray scale (time-division gray scale) is used when a high display quality is not particularly needed while analog grayscale is used when a high display quality is needed as in the case of movies or the like. Furthermore, when information is displayed only in black and white, as in the case of text or the like, the scanning-line driving circuit 12 and the data-line driving circuit 13 may be controlled so that the digital data VDGDATA1 to VDGDATAm is supplied but time-

division gray scale is not executed.

[0089]

When exercising time-division gray scale, in order to represent the image data D of one frame by the organic EL display 10, the control circuit 14 divides one frame into six, and represents one image in 64 levels using the resulting six subframes SF1 to SF6.

[0090]

For the image data D of one frame, the control circuit 14 generates digital data VDGDATA1 to VDGDATAm to be supplied to the individual pixel circuits 20 on the scanning lines Y1 to Yn associated with the first to sixth subframes SF1 to SF6 to the data-line driving circuit 13. At this time, in the first subframe SF1, the control circuit 14 generates digital data VDGDAT1 to VDGDATAm for representing a gray scale of "1". In the second subframe SF2, the control circuit 14 generates digital data VDGDAT1 to VDGDATAm for representing a gray scale of "2". In the third subframe SF3, the control circuit 14 generates digital data VDGDAT1 to VDGDATAm for representing a gray scale of "4". In the fourth subframe SF4, the control circuit 14 generates digital data VDGDAT1 to VDGDATAm for representing a gray scale of "8". In the fifth subframe SF5, the control circuit 14 generates digital data VDGDAT1 to VDGDATAm for representing a gray scale of "16". In the sixth subframe

SF6, the control circuit 14 generates digital data VDGDAT1 to VDGDATAm for representing a gray scale of "32".

[0091]

Then, the control circuit 14 outputs the digital data VDGDATA1 to VDGDATAm of the first to sixth subframes SF1 to SF6 to the digital-data-voltage output circuit 13a of the data-line driving circuit 13 at specific timings. At this time, the control circuit 14 outputs a first control signal SG1 to the first switch Q11 of the data-line driving circuit 13.

[0092]

When digital gray scale is exercised, the control circuit 14 controls timings of sequentially outputting scanning signals SC11 to SCn1 generated by the scanning-line driving circuit 12 for controlling the pixel circuits 20 by sequentially selecting the scanning lines.

[0093]

Furthermore, the control circuit 14 controls timings of sequentially outputting scanning signals SC13 to SCn3 to the scanning lines Y1 to Yn in the subframes SF1 to SF6 by the scanning-line driving circuit 12. In the first subframe SF1, the scanning-line driving circuit 12 outputs the scanning signals SC13 to SCn3 after elapse of the period TL1 from the output of the scanning signals SC11 to SCn1. In the second subframe SF2 and the third subframe SF3, the

control circuit 14 outputs the scanning signals SC13 to SCn3 after elapse of the period TL2 (= 2 × TL1) since the output of the scanning signals SC11 to SCn1 and after elapse of the period TL3 (= 4 × TL1) since the output of the scanning signals SC11 to SCn1, respectively. In the fourth subframe SF4, the fifth subframe SF5, and the sixth subframe SF6, the control circuit 14 outputs the scanning signals SC13 to SCn3 after elapse of the period TL4 (= 8 × TL1) since the output of the scanning signals SC11 to SCn1, after elapse of the period TL5 (= 16 × TL1) since the output of the scanning signals SC11 to SCn1, and after elapse of the period TL6 (= 32 × TL1) since the output of the scanning signals SC11 to SCn1, respectively.

[0094]

When analog gray scale is exercised, the control circuit 14 represents the image data D of one frame by the organic EL display 10. For this purpose, for each of the scanning lines Y1 to Yn selected sequentially, the control circuit 14 generates analog data currents IANDATA1 to IANDATAm for the pixel circuits 20 connected to the scanning line on the basis of the image data D of one frame. The control circuit 14 outputs the analog data currents IANDATA1 to IANDATAm to the analog-data-current output circuit 13b of the data-line driving circuit 13 at specific timings. At this time, the control circuit 14 outputs a second control

signal SG2 to the second switch Q12 of the data-line driving circuit 13.

[0095]

When analog gray scale is exercised, the control circuit 14 controls timings of sequentially outputting scanning signals SC11 to SCn1 and SC12 to SCn2 generated by the scanning-line driving circuit 12 for controlling the pixel circuits 20 by sequentially selecting the scanning lines.

[0096]

Now, an operation of the organic EL display 10 configured as described above will be described.

When the image data D is input from an external device, the control circuit 14 determines whether the image data D represents a still picture that does not require multi-level display or moving-picture data that requires multi-level display. When the image data D is still-picture data, digital gray scale mode is used. When the image data D is moving-picture data, analog gray scale mode is used.

[0097]

(Digital gray scale mode)

First, the digital gray scale mode will be described. For the image data D of one frame, the control circuit 14 generates digital data VDGDATA1 to VDGDATAm to be supplied to the individual pixel circuits 20 on the scanning lines Y1

to Yn associated with the first to sixth subframes SF1 to SF6 to the data-line driving circuit 13. Then, the control circuit 14 outputs the digital data VDGDATA1 to VDGDATAm of the first to sixth subframes SF1 to SF6 to the digital-data-voltage output circuit 13a of the data-line driving circuit 13 at specific timings. At this time, the control circuit 14 outputs the first control signal SG1 to the first switch Q11 of the data-line driving circuit 13.

[0098]

Furthermore, the control circuit 14 controls timings of sequentially outputting the scanning signals SC11 to SCn1, SC12 to SCn2, and SC13 to SCn3 for controlling the pixel circuits 20 by sequentially selecting the scanning lines, generated by the scanning-line driving circuit 12. The scanning-line driving circuit 12 sequentially outputs the first scanning signals SC11 to SCn1 at H level for the first subframe SF1 to sequentially select the first subscanning lines Y11 to Yn1. Furthermore, the scanning-line driving circuit 12 outputs the third scanning signals SC13 to SCn3 after elapse of the period TL1 from the output of the first scanning signals SC11 to SCn1, respectively.

[0099]

Each time one of the scanning lines Y1 to Yn is selected, the data-line driving circuit 13 sequentially output digital data VDGDATA1 to VDGDATAm in the first

subframe SF1 to the pixel circuits 20 on the selected scanning line. Thus, the pixel circuits 20 on the selected scanning line operate (on or off) according to the digital data VDGDATA1 to VDGDATAm. Then, the pixel circuits 20 are sequentially turned off in response to the third scanning signals SC13 to SCn3 at H level after elapse of the period TL1.

[0100]

After supplying digital data VDGDATA1 to VDGDATAm to the pixel circuits 20 on the last scanning line Yn in the first subframe SF1, the scanning-line driving circuit 12 sequentially outputs the first scanning signals SC11 to SCn1 at H level for the second subframe SF2 to sequentially select the first subscanning lines Y11 to Yn1. Furthermore, the scanning-line driving circuit 12 outputs the third scanning signals SC13 to SCn3 after elapse of the period TL2 (= 2 × TL1) from the output of the first scanning signals SC11 to SCn1, respectively.

[0101]

On the other hand, similarly to the case described earlier, the data-line driving circuit 13 sequentially output digital data VDGDATA1 to VDGDATAm in the second subframe SF2 to the pixel circuits 20 on the selected scanning line. Thus, the pixel circuits 20 on the selected scanning line operate (on or off) according to the digital

data VDGDATA1 to VDGDATAm. Then, the pixel circuits 20 are sequentially turned off in response to the third scanning signals SC13 to SCn3 at H level after elapse of the period TL2. Then, similar operations are repeated in the third to sixth subframes SF3 to SF6, whereby an image of one frame is represented. When the operation for displaying the image of one frame has been finished, an operation for displaying an image of a next frame is executed similarly.

[0102]

(Analog gray scale mode)

Next, the analog gray scale mode will be described. On the basis of the image data D for one frame, for each of the scanning lines Y1 to Yn selected sequentially, the control circuit 14 generates analog data currents IANDATA1 to IANDATAm to be supplied to the individual pixel circuits 20 on the selected scanning line. Then, the control circuit 14 outputs the analog data currents IANDATA1 to IANDATAm to the analog-data-current output circuit 13b of the data-line driving circuit 13 at specific timings. At this time, the control circuit 14 outputs the second control signal SG2 to the second switch Q12 of the data-line driving circuit 13. Furthermore, the control circuit 14 controls timing of sequentially outputting the scanning signals SC11 to SCn1, SC12 to SCn2, and SC13 to SCn3 for sequentially selecting the scanning lines and controlling the pixel circuits 20 on

the selected scanning line, generated by the scanning-line driving circuit 12.

[0103]

The scanning-line driving circuit 12 sequentially outputs the first and second scanning signals SC11 to SCn1 and SC12 to SCn2 at H level to sequentially select the scanning lines Y1 to Yn. Each time one of the scanning lines Y1 to Yn (Y11 to Yn1) is selected, the data-line driving circuit 13 sequentially outputs analog data currents IANDATA1 to IANDATAm to the individual pixel circuits 20 on the selected scanning line. Thus, the organic EL elements 21 of the individual pixel circuits 20 on the selected scanning line emit light at luminance levels corresponding to the analog data currents IANDATA1 to IANDATAm.

[0104]

Now, features of the organic EL display 10 configured as described above will be described below.

According to this embodiment, similarly to the first embodiment described earlier, halftones are represented by digital gray scale when multi-level display is not needed, for example, when displaying text or the like, and halftones are represented by analog gray scale when multi-level display is needed, for example, when displaying an animation or movie. That is, halftones are represented by digital gray scale with low power consumption when a high display

quality is not needed, and halftones are represented by analog gray scale when a high display quality is needed. Accordingly, the organic EL display 10 simultaneously achieves low power consumption and a high display quality.

[0105]

Furthermore, according to this embodiment, digital data VDGDATA1 to VDGDATAm and analog data currents IANDATA1 to IANDATAm are supplied to the pixel circuits 20 via the common data lines X1 to Xm, so that the number of wires provided in the display panel 11 is reduced.

[0106]

In this embodiment, the resetting transistor Q5 is constantly kept turned off in analog gray scale mode. Alternatively, the resetting transistor Q5 may be turned on before writing next analog data currents IANDATA1 to IANDATAm, thereby terminating a light-emitting period.

[0107]

(Second Embodiment)

Next, a second embodiment will be described with reference to Fig. 6. This embodiment is characterized by pixel circuits 20, so that only the pixel circuits 20 will be described for convenience of description.

[0108]

Referring to Fig. 6, the pixel circuit 20 includes a driving transistor Q3, first and second switching

transistors Q31 and Q32, a starting transistor Q34, a resetting transistor Q5, and a hold capacitor C1. The driving transistor Q3 is implemented by a P-channel FET. The first and second switching transistors Q31 and Q32, the starting transistor Q34, and the resetting transistor Q5 are implemented by N-channel FETs.

[0109]

The drain of the driving transistor Q3 is connected to the anode of the organic EL element 21 via the starting transistor Q34, and the source thereof is connected to the power-supply line L1. To the power-supply line L1, a power-supply voltage VOEL for driving the organic EL element 21 is supplied. The hold capacitor C1 is connected between the driving transistor Q3 and the power-supply line L1. Furthermore, the resetting transistor Q5 is connected between the gate of the driving transistor Q3 and the power-supply line L1. Furthermore, the gate of the driving transistor Q3 is connected to the data line Xm via the first switching transistor Q31 and the second switching transistor Q32.

[0110]

A node between the first switching transistor Q31 and the second switching transistor Q32 is connected to the drain of the driving transistor Q3. The gates of the first and second switching transistors Q31 and Q32 are connected

to the first subscanning line Yn1 of the scanning line Yn, and the first scanning signal SCn1 is input from the first subscanning line Yn1. The first switching transistor Q31 and the second switching transistor Q32 are turned on or off according to the first scanning signal SCn1 and the second scanning signal SCn2, respectively, as will be described later. Then, digital data VDGDATAm or an analog data current IANDATAm supplied from the data line Xm as will be described later is supplied to the hold capacitor C1.

[0111]

The gate of the starting transistor Q34 is connected to the second sub-scanning line Yn2 of the scanning line Yn, and the second scanning signal SCn2 is input from the second sub-scanning line Yn2. When the starting transistor Q34 is turned on according to the second scanning signal SCn2 while the driving transistor Q3 is on, a driving current is supplied to the organic EL element 21.

[0112]

The gate of the resetting transistor Q5 is connected to the third sub-scanning line Yn3 of the scanning line Yn, and the third scanning signal SCn3 is input from the third sub-scanning line Yn3. When the resetting transistor Q5 is turned on according to the third scanning signal SCn3, the power-supply voltage VOEL supplied from the power-supply line L1is applied to the first end of the hold capacitor C1

via the resetting transistor Q5. When the power-supply voltage VOEL is applied to the first end of the hold capacitor C1, the hold capacitor C1 is reset, so that the driving transistor Q3 is turned off.

[0113]

In the pixel circuit 20 configured as described above, time-division gray scale is exercised in the following manner so that binary data voltages are written to the pixel circuits 20 associated with one scanning line sequentially selected from the scanning lines while simultaneously starting supply of currents having current levels corresponding to the binary data voltages to the organic EL elements 21 and so that the supply of currents is stopped after a predetermined time. Referring to Fig. 7, in the sub-frames SF1 to SF6, the starting transistor Q34 is kept turned on according to the second scanning signal SCn2 at H level, and the resetting transistor Q5 is kept turned off according to the third scanning signal SCn3 at L level. In this state, the first and second switching transistors Q31 and Q32 are turned on according to the first scanning signal SCn1 at H level.

[0114]

When the first and second switching transistors Q31 and Q32 are turned on, digital data VDGDATAm is supplied to the hold capacitor C1 via the data line Xm. The digital data

VDGDATAm is binary data for setting either a minimum value or a maximum value (or a lower limit value or an upper limit value) of the luminance of the organic EL element 21 similarly to the embodiment described earlier, i.e., binary data for setting the resistance of the driving transistor Q3 to either a minimum value or a maximum value. In the hold capacitor C1 holding the digital data VDGDATAm, even when the first scanning signal SCn1 is pulled to L level so that the first and second switching transistors Q31 and S32 are turned off, the stored digital data VDGDATAm is maintained.

[0115]

Then, the driving transistor Q3 is controlled so as to be turned on or off according to the content of the stored digital data VDGDATAm. When the driving transistor Q3 is on, a driving current is supplied to the organic EL element 21 so that the organic EL element is caused to emit light. On the other hand, when the driving transistor Q3 is off, the supply of a driving current is stopped so that the organic EL element 21 is caused to stop emitting light.

[0116]

Then, when the third scanning signal SCn3 is output to the third sub-scanning line Yn3 at a timing based on the sub-frames SF1 to SF6, the resetting transistor Q5 that has been off is turned on. When the resetting transistor Q5 is turned on, the power-supply voltage VOEL is applied from the

power-supply line L1 to the hold capacitor C1 via the resetting transistor Q5, whereby the digital data VDGDATAm is deleted and the gate of the driving transistor Q3 is pulled to the potential of the power-supply voltage VOEL. That is, the hold capacitor C1 is reset.

[0117]

When the hold capacitor C1 is reset, the driving transistor Q3 is turned off, so that the organic EL element 21 that has been emitting light according to the digital data VDGDATAm stops emitting light, and waits for a next light-emitting operation to be executed. That is, when time-division gray scale is exercised, the light-emitting periods TL1 to TL6 of the organic EL element 21 of the pixel circuit 20 correspond to a period from a time when the first scanning signal SCn1 is output to a time when the third scanning signal SCn3 is output.

[0118]

In the pixel circuit 20, analog gray scale is exercised in the following manner to control the conduction state of the driving transistor Q3 in accordance with a gray scale so that a current having a current level corresponding to a multi-value data current is supplied to the organic EL element 21. Referring to Fig. 8, the first and second switching transistors Q31 and Q32 and the starting transistor Q34 are controlled so as to be turned on and off

at specific timings, whereby analog gray scale is exercised. At this time, the third scanning signal SCn3 is output so that the resetting transistor Q5 is kept turned off.

[0119]

More specifically, when the first scanning signal SCn1 at H level is output to the first sub-scanning line Yn1, the first and second switching transistors Q31 and Q32 are both turned on. Thus, an analog data current IANDATAm is supplied from the data line Xm via the first and second switching transistors Q31 and Q32. Thus, an amount of charge corresponding to the analog data current IANDATAm is held in the hold capacitor C1. Thus, the voltage applied to the gate of the driving transistor Q3 becomes a voltage corresponding to a luminance level that is set according to the analog data current IANDATAm.

[0120]

Then, when the starting transistor 34 is turned on in response to the second scanning signal SCn2, the driving transistor Q3 is turned on in response to the reduced gate voltage, so that a driving current corresponding to the gate voltage is supplied to the organic EL element 21. The organic EL element 21 emits light at a luminance level that is determined according to the driving current supplied thereto.

[0121]

As described above, according to this embodiment, similarly to the first embodiment described earlier, halftones can be represented by digital gray scale when multi-level display is not needed, for example, when displaying text or the like, and halftones can be represented by analog gray scale when multi-level display is needed, for example, when displaying an animation or movie. Thus, halftones can be represented by digital gray scale with low power consumption when a high display quality is not needed, and halftones can be represented by analog gray scale when a high display quality is needed. Accordingly, the organic EL display 10 simultaneously achieves low power consumption and a high display quality.

[0122]

Furthermore, according to the second embodiment, digital data VDGDATA1 to VDGDATAm and analog data currents IANDATA1 to IANDATAm are supplied to the pixel circuits 20 via the common data lines X1 to Xm, so that the number of wires provided in the display panel 11 is reduced.

[0123]

In this embodiment, the resetting transistor Q5 is constantly kept turned off in analog gray scale mode. Alternatively, the resetting transistor Q5 may be turned on before writing next analog data currents IANDATA1 to IANDATAm, thereby terminating a light-emitting period.

[0124]

(Third Embodiment)

Next, a third embodiment will be described with reference to Fig. 9. Since this embodiment is characterized by pixel circuits 20, only the pixel circuits 20 will be described for convenience of description.

[0125]

Referring to Fig. 9, the pixel circuit 20 includes a driving transistor Q3, first and second switching transistors Q41 and Q42, a starting transistor Q44, a compensating transistor Q45 as a third transistor, a resetting transistor Q5, and a hold capacitor C1. The driving transistor Q3 is implemented by a P-channel FET. The first and second switching transistors Q41 and Q42, the starting transistor Q44, the compensating transistor Q45, and the resetting transistor Q5 are implemented by N-channel FETs.

[0126]

The drain of the driving transistor Q3 is connected to the anode of the organic EL element 21, and the source thereof is connected to the power-supply line L1 via the starting transistor Q44. To the power-supply line L1, a power-supply voltage VOEL for driving the organic EL element 21 is supplied. The hold capacitor C1 is connected between the gate of the driving transistor Q3 and the power-supply

line L1. Furthermore, the resetting transistor Q5 is connected between the gate of the driving transistor Q3 and the power-supply line L1.

[0127]

Furthermore, the gate of the driving transistor Q3 is connected to the data line Xm via the first switching transistor Q41. Furthermore, the source of the driving transistor Q3 is connected to the data line Xm via the second switching transistor Q42. The compensating transistor Q45 is connected between the gate and drain of the driving transistor Q3.

[0128]

The gate of the first switching transistor Q41 is connected to a fifth sub-scanning line Yn5 of the scanning line Yn, and a fifth scanning signal SCn5 is input from the fifth sub-scanning line Yn5. When the first switching transistor Q41 is turned on or off according to the fifth scanning signal SCn5 as will be described later, digital data VDGDATAm or an analog data current IANDATAm supplied from the data line Xm as will be described later is supplied to the hold capacitor C1.

[0129]

The gate of the second switching transistor Q42 is connected to the first sub-scanning line Yn1 of the scanning line Yn, and the first scanning signal SCn1 is input from

the first sub-scanning line Yn1. When the second switching transistor Q42 is turned on according to the first scanning signal SCn1, a voltage having the same potential as the power-supply voltage VOEL is applied to the source of the driving transistor Q3 from the data line Xm. More specifically, in the case of analog gray scale, before an analog data current IANDATAm is output from the analog-data-current output circuit 13b, a bias voltage having the same potential as the power-supply voltage VOEL is applied to the data line Xm by a supplying circuit that is not shown.

[0130]

The gate of the starting transistor Q44 is connected to the third sub-scanning line Yn3 of the scanning line Yn, and the third scanning signal SCn3 is input from the third sub-scanning line Yn3. When the starting transistor Q44 is turned on according to the third scanning signal SCn3 while the driving transistor Q3 is on, a driving current is supplied to the organic EL element 21. The gate of the compensating transistor Q45 is connected to the second subscanning line Yn2 of the scanning line Yn, and the second scanning signal SCn2 is input from the second subscanning line Yn2. In the case of analog gray scale, when the compensating transistor Q45 is turned on according to the second scanning signal SCn2, a current that flows through the driving transistor Q3 in accordance with a bias voltage

having the same potential as the power-supply voltage VOEL is supplied from the data line Xm to the hold capacitor C1.

[0131]

The gate of the resetting transistor Q5 is connected to a fourth sub-scanning line Yn4 of the scanning line Yn, and a fourth scanning signal SCn4 is input from the fourth sub-scanning line Yn4. When the resetting transistor Q5 is turned on according to the fourth scanning signal SCn4, the power-supply voltage VOEL supplied via the power-supply line L1 is applied to the first end of the hold capacitor C1 via the resetting transistor Q5. When the power-supply voltage VOEL is applied to the first end of the hold capacitor C1, the hold capacitor C1 is reset, whereby the driving transistor Q3 is turned off.

[0132]

In the pixel circuit 20 configured as described above, time-division gray scale is exercised in the following manner so that binary data voltages are written to the pixel circuits 20 associated with one scanning line sequentially selected from the scanning lines while simultaneously starting supply of currents having current levels corresponding to the binary data voltages to the organic EL elements 21 and so that the supply of currents is stopped after a predetermined time.

[0133]

Referring to Fig. 10, in the subframes SF1 to SF6, the starting transistor Q44 is kept turned on according to the third scanning signal SCn3 at H level. Furthermore, the second switching transistor Q42 and the compensating transistor Q45 are kept turned off according to the first and second scanning signals SCn1 and SCn2 at L level. Furthermore, the resetting transistor Q5 is kept turned off according to the fourth scanning signal SCn4 at L level. In this state, the first switching transistor Q41 is turned on according to the fifth scanning signal SCn5 at H level.

[0134]

When the first switching transistor Q41 is turned on, digital data VDGDATAm is supplied from the data line Xm to the hold capacitor C1. Similarly to the embodiments described earlier, the digital data VDGDATAm is used to set either a minimum value or a maximum value (or a lower limit value or an upper limit value) of the luminance of the organic EL element 21, i.e., data for setting the resistance of the driving transistor Q3 to either a minimum value or a maximum value. The hold capacitor C1 holding the digital data VDGDATAm maintains the stored digital data VDGDATAm even when the fifth scanning signal SCn5 is pulled to L level so that the first switching transistor Q41 is turned off.

[0135]

The driving transistor Q3 is controlled so as to be turned on or off according to the stored digital data VDGDATAm. When the driving transistor Q3 is on, a driving current is supplied to the organic EL element 21 so that the organic EL element 21 is caused to emit light. On the other hand, when the driving transistor Q3 is off, the supply of a driving current is stopped so that the organic EL element 21 is caused to stop emitting light.

[0136]

Then, when the fourth scanning signal SCn4 is output to the fourth sub-scanning line Yn4 at a timing based on the sub-frames SF1 to SF6, the resetting transistor Q5 that has been off is turned on. When the resetting transistor Q5 is turned on, the power-supply voltage VOEL is applied from the power-supply line L1 to the hold capacitor C1 via the resetting transistor Q5, whereby the digital data VDGDATAm is deleted and the gate of the driving transistor Q3 is pulled to the potential of the power-supply voltage VOEL. That is, the hold capacitor C1 is reset.

[0137]

When the hold capacitor C1 is reset, the driving transistor Q3 is turned off, whereby the organic EL element 21 that has been emitting light according to the digital data VDGDATAm stops emitting light, and waits for a next light-emitting operation to be executed. That is, when

time-division gray scale is exercised, the light-emitting periods TL1 to TL6 of the organic EL element 21 of the pixel circuit 20 correspond to a period from a time when the first scanning signal SCn1 is output to a time when the third scanning signal SCn3 is output.

[0138]

In the pixel circuit 20, analog gray scale is exercised in the following manner to control the conduction state of the driving transistor Q3 in accordance with a gray scale so that a current having a current level corresponding to a multi-value data current is supplied to the organic EL element 21. Referring to Fig. 11, the resetting transistor Q5 is kept turned off according to the fourth scanning signal SCn4 at L level. The second switching transistor Q42, the starting transistor Q44, and the compensating transistor Q45 are controlled so as to be turned on and off at specific timings by outputting the first to third and fifth scanning signals SCn1 to SCn3 and SCn5, whereby analog gray scale is exercised.

[0139]

That is, the scanning signal SCn1 at H level is output to the first subscanning line Yn1 with the resetting transistor S5 kept turned off, the second switching transistor Q42 is turned on. At this time, the bias voltage (= VOEL) applied to the data line Xm is applied to the

source of the driving transistor Q3 via the second switching transistor Q42. At this time, the driving transistor Q3 is on due to an amount of charge corresponding to the analog data current IANDATAm stored in the hold capacitor C1 in a previous cycle (before output of the scanning signal SCn1 at H level), so that a current flows through the organic EL element 21. Thus, the potential at the drain of the driving transistor Q3 is sufficiently close to the ground potential of the organic EL element 21. Accordingly, the potential at the drain of the driving transistor Q3 has a sufficient negative amplitude, so that the driving transistor Q3 is ensured to be open.

[0140]

Then, when the scanning signal SCn2 output to the second subscanning line Yn2 is pulled from L level to H level, the compensating transistor Q45 is turned on. Furthermore, the scanning signal SCn3 on the third subscanning line Yn3 is lost (is pulled to L level), so that the starting transistor Q44 is turned off.

[0141]

When the compensating transistor is turned on and the starting transistor is turned off, a current caused by the bias voltage is supplied to the gate of the driving transistor Q3, raising the potential at the gate. When the gate voltage of the driving transistor Q3 is raised to a

voltage (= VOEL - Vth) obtained by subtracting a threshold voltage Vth of the driving transistor Q3 from the bias voltage (= VOEL), the driving transistor is turned off. Then, when the scanning signal SCn2 on the second subscanning line Yn2 is pulled to L level, the compensating transistor Q45 is turned off. At this time, the gate voltage of the driving transistor Q3 is maintained at the voltage (= VOEL - Vth) obtained by subtracting the threshold voltage Vth of the driving transistor Q3 from the bias voltage (= VOEL).

[0142]

When the gate voltage of the driving transistor Q3 is maintained at the voltage (= VOEL - Vth), the fifth scanning signal SCn5 at H level is output to the fifth subscanning line Yn5, and the scanning signal SCn1 at H level is lost (L level). Thus, the first switching transistor Q41 is turned on, so that an analog data current IANDATAm is supplied from the data line Xm. At this tie, since the driving transistor Q3 and the compensating transistor Q45 are off, the amount of charge in the hold capacitor C1 decreases in accordance with the analog data current IANDATAm. That is, the gate voltage of the driving transistor Q3 decreases in accordance with the analog data current IANDATAm. In this state, the scanning signal SCn5 on the fifth subscanning line Yn5 is pulled to L level, so that the first switching transistor

Q41 is turned off. When the switching transistor Q41 is turned off, the gate voltage of the driving transistor Q3 is maintained at the potential reduced in accordance with the analog data current IANDATAm.

[0143]

Then, the scanning signal SCn3 at H level is output from the third subscanning line Yn3, so that the starting transistor Q44 is turned on. When the starting transistor Q44 is turned on, the driving transistor Q3 exhibits a conduction state corresponding to the value of the analog data current IANDATAm, so that a driving current corresponding to the analog data current IANDATAm is supplied to the organic EL element 21. The organic EL element 21 emits light at a luminance level corresponding to the analog data current IANDATAm.

[0144]

As described above, according to this embodiment, similarly to the first and second embodiments described earlier, halftones can be represented by digital gray scale when multi-level display is not needed, for example, when displaying text or the like, and halftones can be represented by analog gray scale when multi-level display is needed, for example, when displaying an animation or movie. Thus, halftones can be represented by digital gray scale with low power consumption when a high display quality is

not needed, and halftones can be represented by analog gray scale when a high display quality is needed. Accordingly, the organic EL display 10 simultaneously achieves low power consumption and a high display quality.

[0145]

Furthermore, according to the third embodiment, digital data VDGDATA1 to VDGDATAm and analog data currents IANDATA1 to IANDATAm are supplied to the pixel circuits 20 via the common data lines X1 to Xm, so that the number of wires provided in the display panel 11 is reduced.

[0146]

In this embodiment, the resetting transistor Q5 is constantly kept turned off in analog gray scale mode. Alternatively, the resetting transistor Q5 may be turned on before writing next analog data currents IANDATA1 to IANDATAm, thereby terminating a light-emitting period.

[0147]

(Fourth Embodiment)

Next, an embodiment of an electronic apparatus including the organic EL display 10 as an electro-optical device according to the first embodiment will be described with reference to Figs. 12 and 13. The organic EL display 10 can be applied to various electronic apparatuses, such as mobile personal computers, cellular phones, and digital cameras.

[0148]

Fig. 12 is a perspective view showing the configuration of a mobile personal computer. Referring to Fig. 12, a personal computer 60 includes a main unit 62 having a keyboard 61, and a display unit 63 including the organic EL display 10. Also in this case, the display unit 63 including the organic EL display 10 exhibits the same advantages as in the embodiments described earlier. Thus, the personal computer 60 simultaneously achieves low power consumption and adequate display quality.

[0149]

Fig. 13 is a perspective view showing the configuration of a cellular phone. Referring to Fig. 13, a cellular phone 70 includes a plurality of operating buttons 71, an earpiece 72, a mouthpiece 73, and a display unit 74 including the organic EL display 10. Also in this case, the display unit 74 including the organic EL display 10 exhibits the same advantages as in the embodiments described earlier. Thus, the cellular phone 70 simultaneously achieves low power consumption and adequate display quality.

[0150]

The embodiments of the present invention can be modified as follows.

• In the first to third embodiments described above, either analog gray scale or digital gray scale is used on

the basis of whether image data to be displayed does not require multi-level display, as in the case of text or the like, or requires multi-level display, as in the case of animations or movies. Alternatively, it is possible to use digital gray scale when low power consumption is desired while using analog gray scale when low power consumption need not be considered, without distinction among text, animation, and movies. Yet alternatively, it is possible to use digital gray scale when a lower display quality is desired while using analog gray scale when a higher display quality is desired, without distinction among text, animation, and movies.

[0151]

• In the first to third embodiments described above, digital gray scale is implemented by time-division gray scale in which binary data voltages are written to the pixel circuits 20 associated with one scanning line sequentially selected from the scanning lines while simultaneously starting supply of currents having current levels corresponding to the binary data voltages to the organic EL elements 21 and the supply of currents is stopped after a predetermined time.

[0152]

Alternatively, the arrangement may be such that data voltages are written to all the pixel circuits with a

reverse bias applied to an opposing electrode of the organic EL elements 21, a forward bias is applied to the opposing electrode of the organic EL elements 21 after the writing is finished to cause light emission, and the reverse bias is applied again at the end of each subframes. Furthermore, digital gray scale may be implemented by area gray scale. More specifically, with each pixel circuit 20 as a subpixel, a plurality of subpixels is grouped. When exercising digital gray scale, halftones are represented by exercising control so that an appropriate number of subpixels belonging to the group emit light and the other subpixels do not emit light.

[0153]

• In the first to third embodiments described above, digital data VDGDATA1 to VDGDATAm and analog data currents IANDATA1 to IANDATAm are supplied to the pixel circuits 20 via the common data lines X1 to Xm. Alternatively, separate data lines may be provided.

[0154]

• In the embodiments described above, favorable advantages are achieved using the pixel circuit 20 as an electronic circuit. Alternatively, the present invention may be applied to an electronic circuit for driving an electro-optical element other than the organic EL element 21, for example, an LED or an FED.

[0155]

Although the organic EL elements 21 are used in the embodiments described above, inorganic EL elements may be used. That is, the present invention may be applied to an inorganic EL display including inorganic EL elements.

[0156]

[Advantages]

According to the present invention, low power consumption and adequate display quality can be achieved simultaneously.

[Brief Description of the Drawings]

[Fig. 1]

Fig. 1 is a block circuit diagram showing the circuit configuration of an organic EL display for explaining a first embodiment.

[Fig. 2]

Fig. 2 is a circuit diagram showing the internal circuit configuration of a pixel circuit and a data-line driving circuit.

[Fig. 3]

Fig. 3 is a diagram for explaining sequential turn-on and simultaneous turn-off in time-division gray scale.

[Fig. 4]

Fig. 4 is a timing chart for explaining selection of a scanning line for exercising time-division gray scale.

[Fig. 5]

Fig. 5 is a timing chart for explaining selection of a scanning line for exercising analog gray scale.

[Fig. 6]

Fig. 6 is a circuit diagram for explaining the internal circuit configurations of a pixel circuit and a data-line driving circuit for explaining a second embodiment.

[Fig. 7]

Fig. 7 is a timing chart for explaining selection of a scanning line for exercising time-division gray scale in the second embodiment.

[Fig. 8]

Fig. 8 is a timing chart for explaining selection of a scanning line for exercising analog gray scale in the second embodiment.

[Fig. 9]

Fig. 9 is a circuit diagram for explaining the internal circuit configurations of a pixel circuit and a data-line driving circuit for explaining a third embodiment.

[Fig. 10]

Fig. 10 is a timing chart for explaining selection of a scanning line for exercising time-division gray scale in the third embodiment.

[Fig. 11]

Fig. 11 is a timing chart for explaining selection of a

scanning line for exercising analog gray scale in the third embodiment.

[Fig. 12]

Fig. 12 is a perspective view showing the configuration of a mobile personal computer for explaining a fourth embodiment.

[Fig. 13]

Fig. 13 is a perspective view showing the configuration of a cellular phone for explaining the fourth embodiment.

[Reference Numerals]

10: organic EL display as electro-optical device

11: display panel

12: data-line driving circuit

13: scanning-line driving circuit

14: control circuit as controlling means

20: pixel circuit as electronic circuit or unit circuit

21: organic EL element as electronic element or electro-optical element

13a: digital-data-voltage output circuit as data-voltage output circuit

13b: analog-data-current output circuit as data-current output circuit

Y1 to Yn: scanning lines

X1 to Xm: data lines

SCn: scanning signal

D: image data

VDGDATA1 to VDGDATAm: digital data as binary data voltages

IANDATA1 to IANDATAm: analog data currents as multi-value data currents

[Name of Document] ABSTRACT

[Abstract]

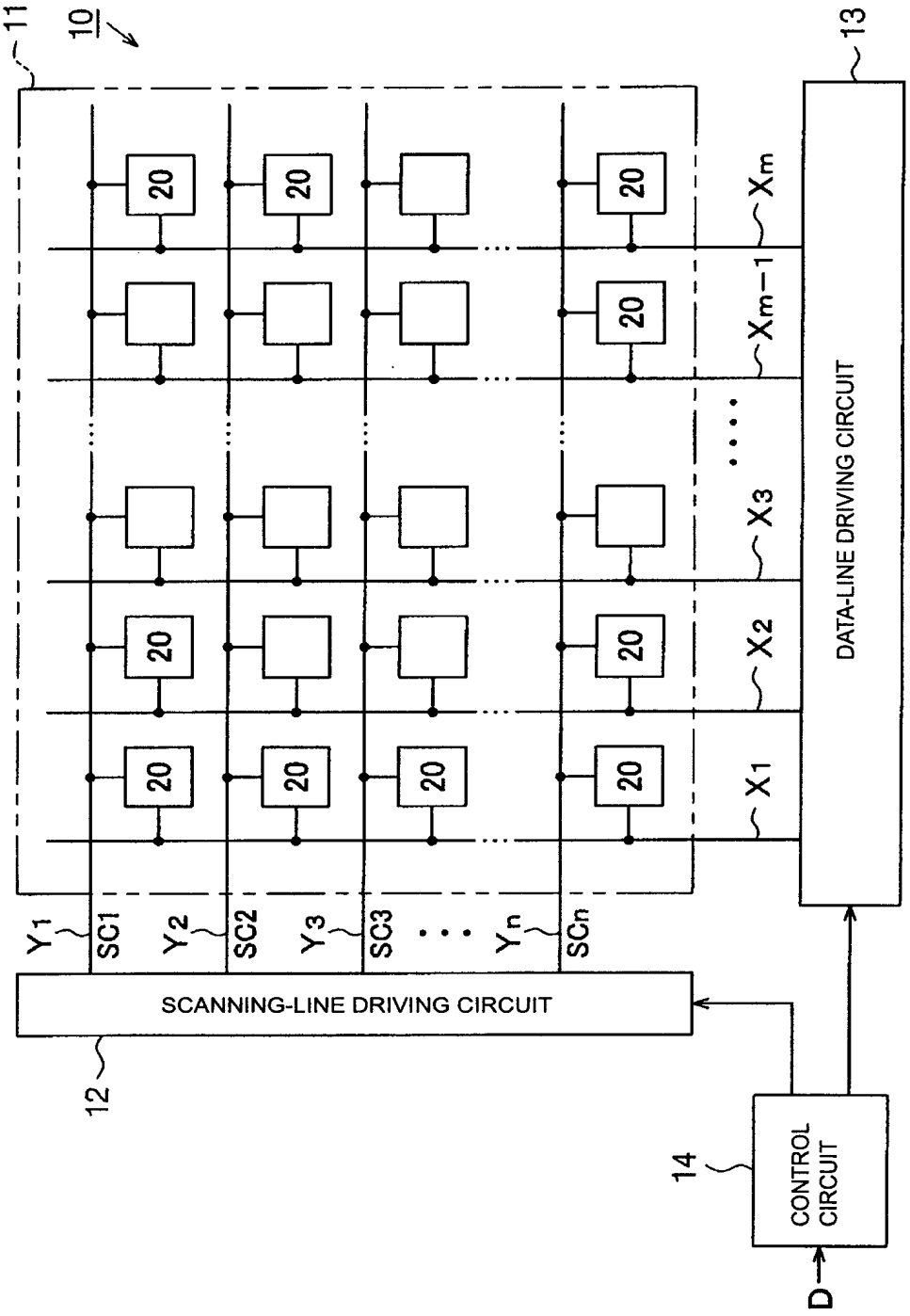
[Object] To provide an electronic circuit, an electro-optical device, a method of driving an electro-optical device, and an electronic apparatus with which low power consumption and adequate display quality can be achieved simultaneously.

[Solving Means] To an organic EL element 21 of a pixel circuit 20 provided in association with an intersection of a scanning line Yn and a data line Xm, a driving current corresponding to digital data VDGDATAm or an analog data current IANDATAm is supplied via the data line Xm. When halftones are controlled by digital gray scale in order to reduce power consumption, the digital data VDGDATAm having a value corresponding to either H level or L level is supplied to the pixel circuit 20. When halftones are controlled by analog gray scale in order to improve display quality, the analog data current IANDATAm is supplied to the pixel circuit 20.

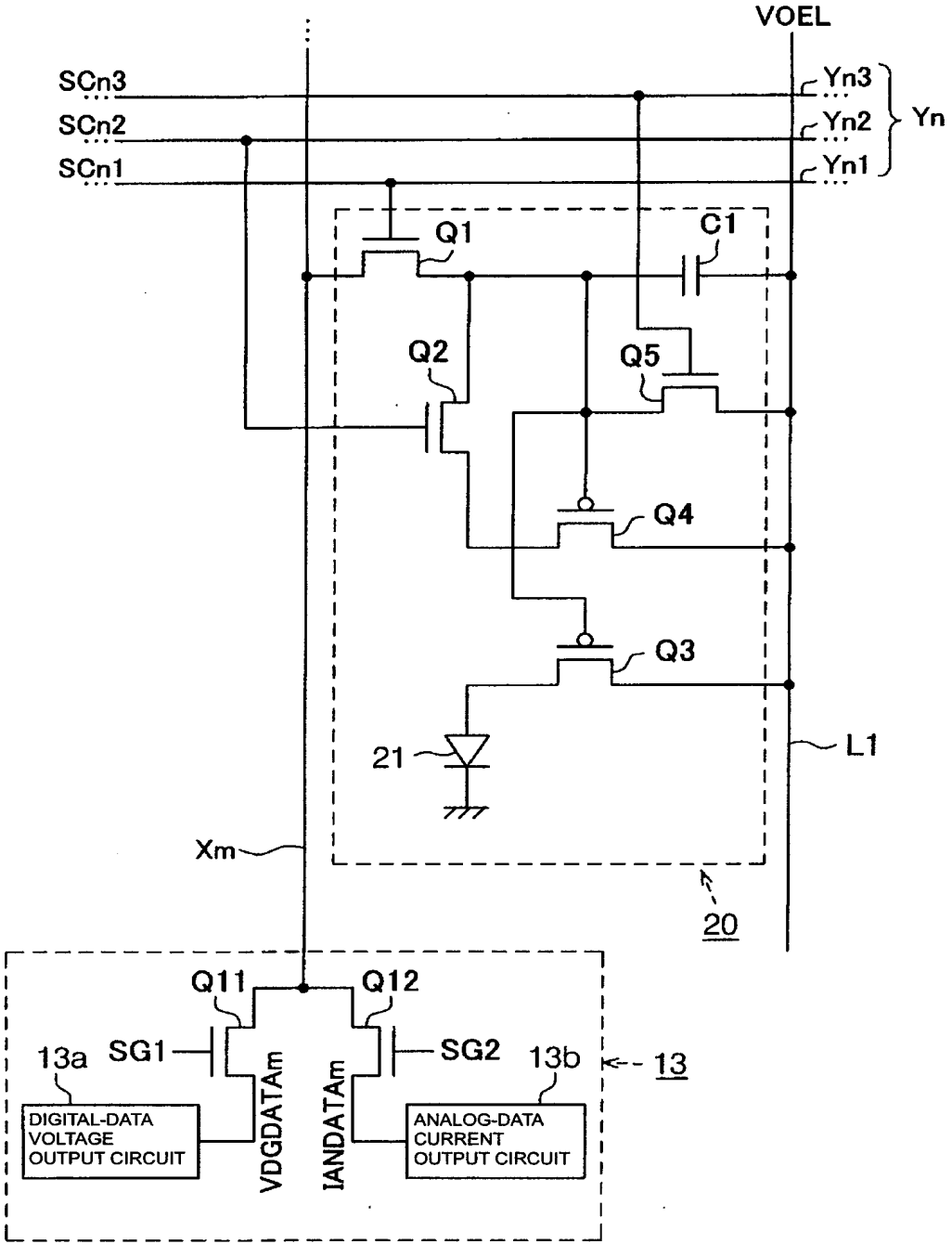
[Selected Figure] Fig. 2

[Name of Document] DRAWINGS

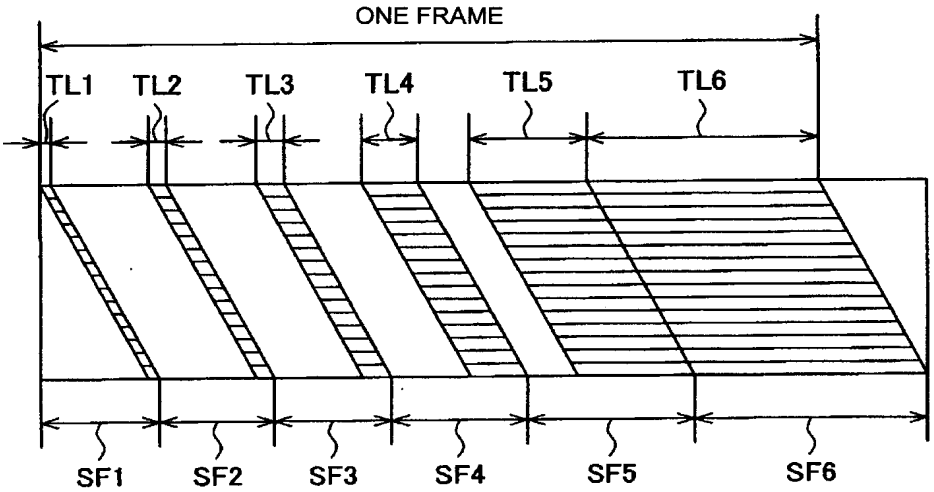
[FIG. 1]



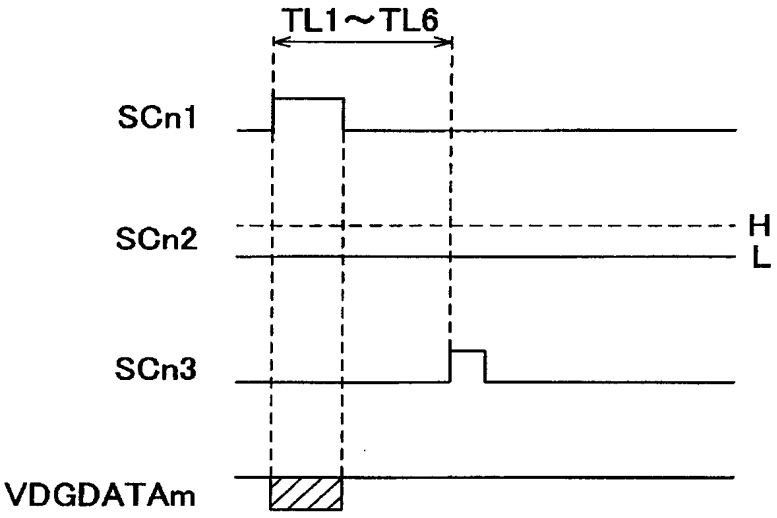
[FIG. 2]


VOEL
SCn3
SCn2
SCn1
Yn3
Yn2
Yn1
Yn
Q1
C1
Q2
Q5
Q4
Q3
21
L1
Xm
20
Q11
Q12
13a
SG1
SG2
13b
13
DIGITAL-DATA VOLTAGE OUTPUT CIRCUIT
VDGDATAm
IANDATAm
ANALOG-DATA CURRENT OUTPUT CIRCUIT

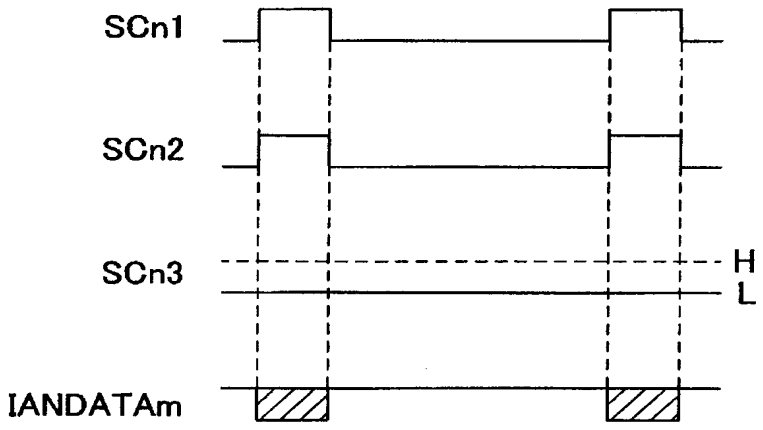
[FIG. 3]



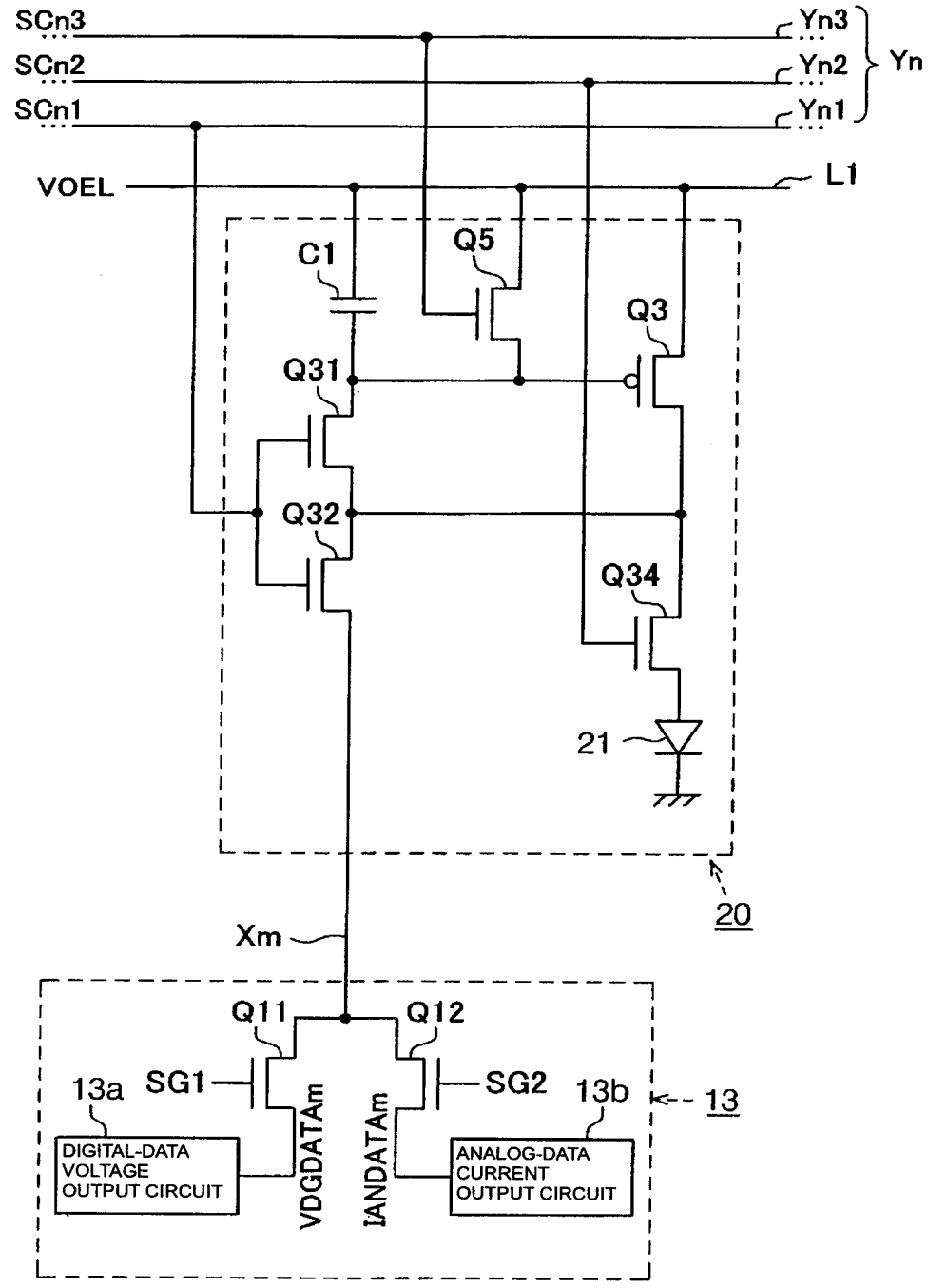
[FIG. 4]


TL1~TL6
SCn1
SCn2
H
L
SCn3
VDGDATAm

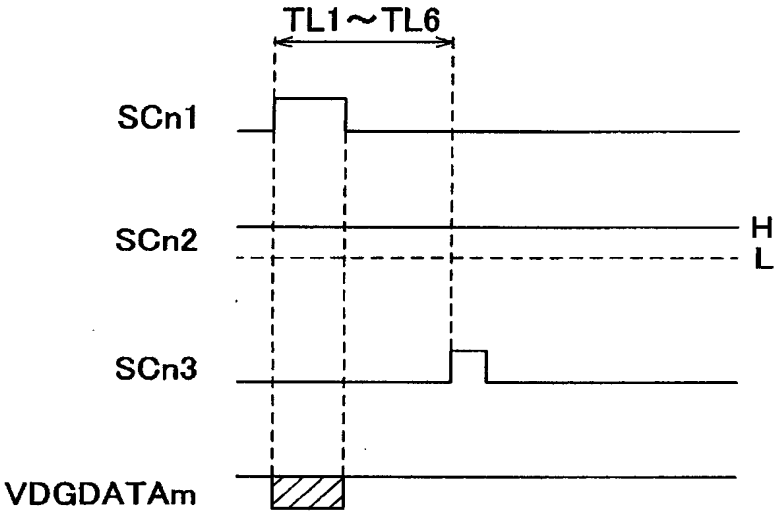
[FIG. 5]


SCn1
SCn2
SCn3
H
L
IANDATAm

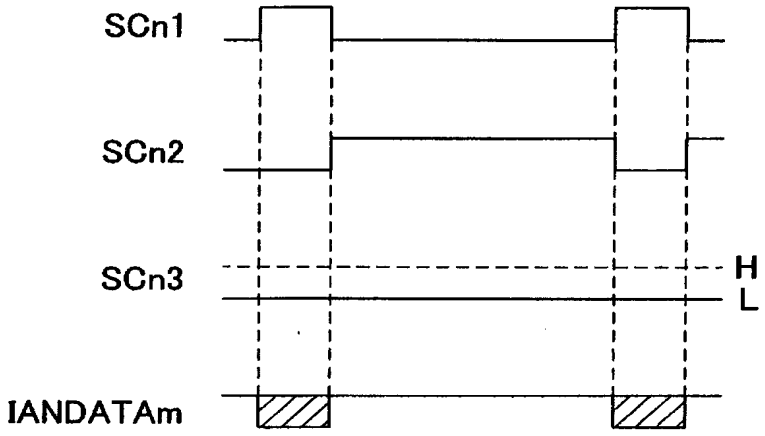
[FIG. 6]


SCn3
SCn2
SCn1
Yn3
Yn2
Yn1
Yn
VOEL
L1
C1
Q5
Q3
Q31
Q32
Q34
21
20
Xm
Q11
Q12
13a
SG1
SG2
13b
13
DIGITAL-DATA VOLTAGE OUTPUT CIRCUIT
ANALOG-DATA CURRENT OUTPUT CIRCUIT
VDGDATAm
IANDATAm

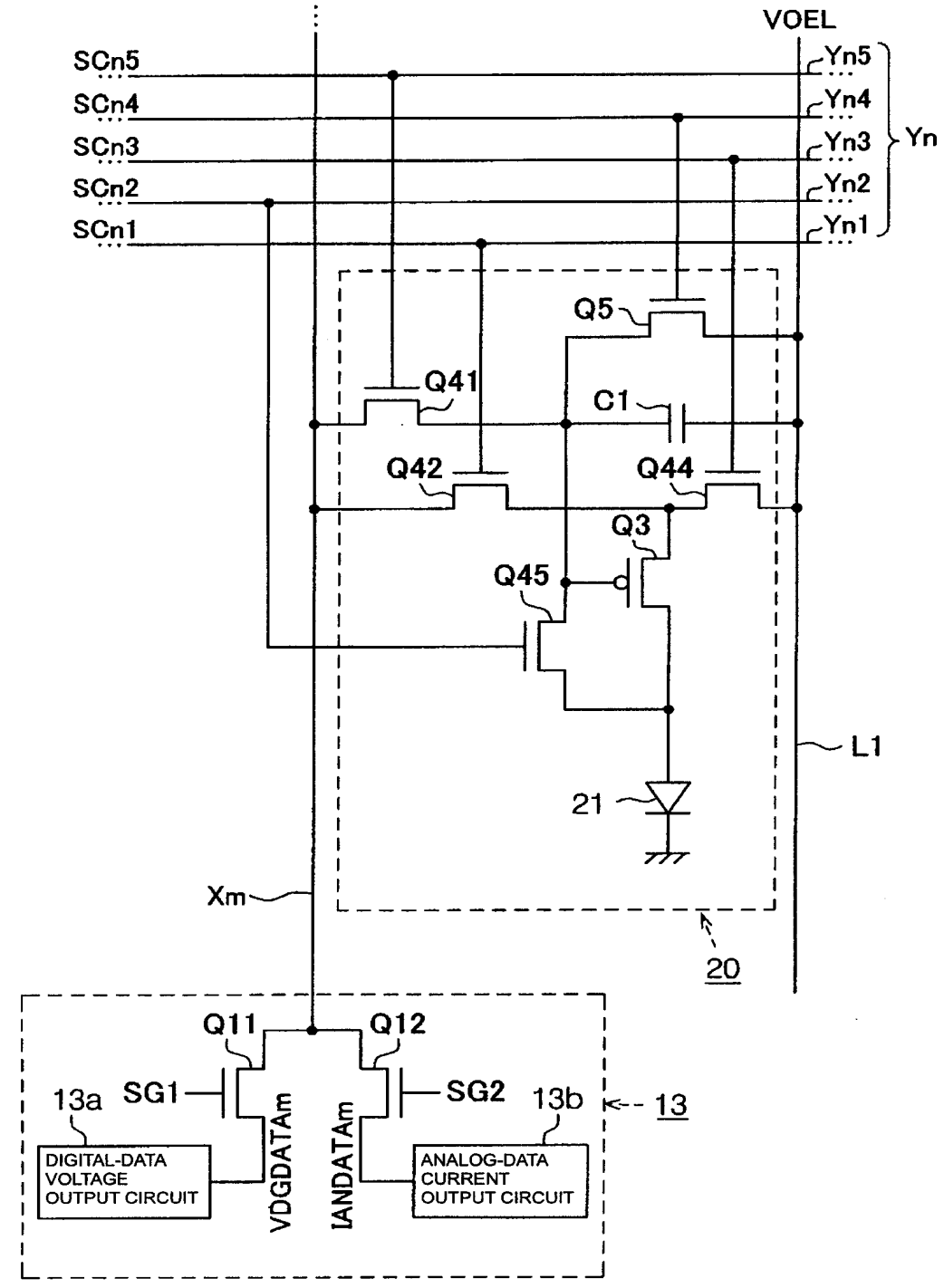
[FIG. 7]


TL1~TL6
SCn1
SCn2
H
L
SCn3
VDGDATAm

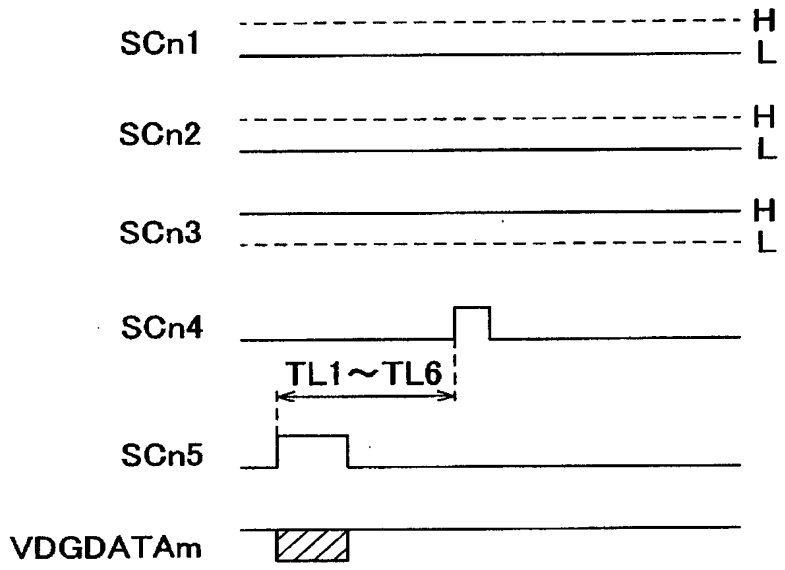
[FIG. 8]


SCn1
SCn2
SCn3
H
L
IANDATAm

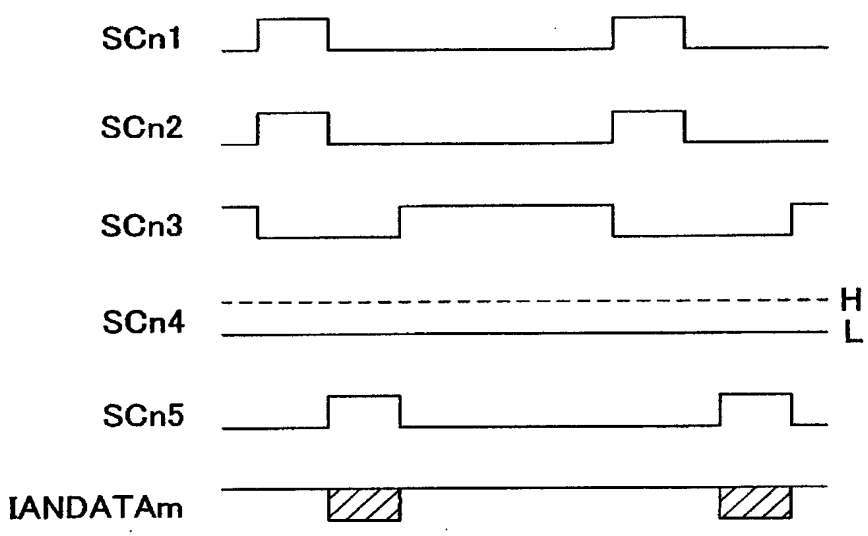
[FIG. 9]


VOEL
SCn5
SCn4
SCn3
SCn2
SCn1
Yn5
Yn4
Yn3
Yn2
Yn1
Yn
Q5
Q41
C1
Q42
Q44
Q3
Q45
L1
21
Xm
20
Q11
Q12
13a
SG1
SG2
13b
13
DIGITAL-DATA VOLTAGE OUTPUT CIRCUIT
VDGDATAm
IANDATAm
ANALOG-DATA CURRENT OUTPUT CIRCUIT

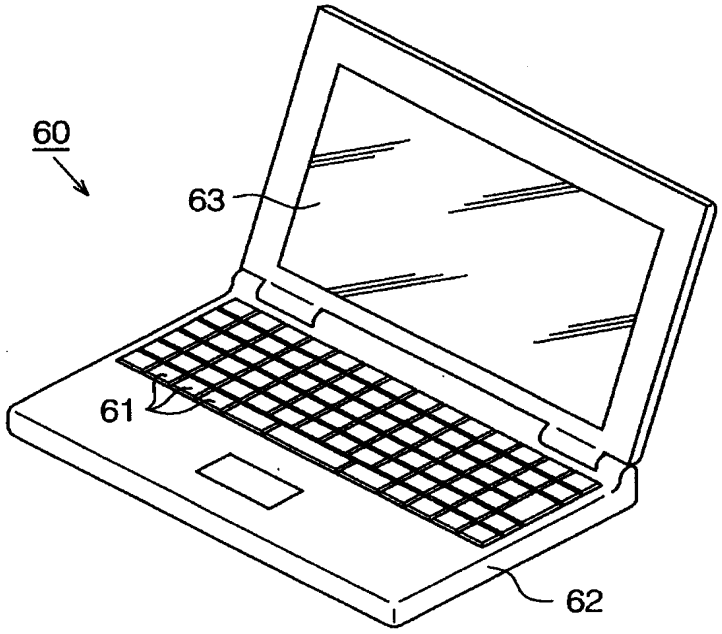
[FIG. 10]


SCn1
H
L
SCn2
H
L
SCn3
H
L
SCn4
TL1~TL6
SCn5
VDGDATAm

[FIG. 11]


SCn1
SCn2
SCn3
SCn4
H
L
SCn5
IANDATAm

[FIG. 12]



[FIG. 13]